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NOTES:
1.HSF Property:Comply iSupplier system HSF property attribute up-to-date value.

CPU LIST			
I3-1005G1	ICL	6025B0405601	SRGKF
I5-1035G1	ICL	6025B0404801	SRGKG
I7-1065G7	ICL	6025B0407701	SRGON

GPU LIST		
AMD R19M-M18-30	GDDR5 216-0915020	6019B1961001

VRAM LIST		
Hynix	H5GC8H24MJR-R0C	6019B1542101
Micron	MT51J256M32HF-70:A	6019B1486001
Samsung	K4G80325FB-HC28	6019B1485901
Hynix	H5GC8H24AJR-R2C A	6019B1723701
Micron	MT51J256M32HF-80:B B	6019B1721101
Samsung	K4G80325FC-HC25	6019B1926601

HEDWIG

INTEL ICE LAKE-U 15W

DIS : 24.5X24.5

GPU : AMD R19M-M18-30

VRAM : GDDR5 256MX32X2PCS

MV BUILD 2020.01.07

SSID
UMA 868C
DIS 868D

LOCATION	LEVEL	CO-LAY
PAD6015	PVBAT	SHORT
PAD60200	P5V0A	SHORT
PAD60210	PVBAT	SHORT
PAD60100	P3V3A	SHORT
PAD60110	PVBAT	SHORT
PAD60103	P3V3AL	SHORT
PAD60310	PVBAT	SHORT
PAD60300	P1V2	SHORT
PAD60350	P0V6S	SHORT
PAD6970	P1V8A	SHORT R6979 OPEN
PAD6980	P5V0A	SHORT
PAD66020	PVBAT	SHORT
PAD66010	PVBAT	SHORT
PAD66610	PVBAT	SHORT
PAD60410	P3V3A	SHORT
PAD3000	PVBAT	OPEN F3033 SHORT
PAD67010	PVBAT	SHORT
PAD67200	P1V35S_DGPU	SHORT
PAD67210	PVBAT	SHORT
PAD67500	PVPCIE	SHORT
PAD67510	P3V3A	SHORT
PAD67410	P3V3A	SHORT
PAD67400	P1V8S_DGPU	SHORT
PAD1700	P5V0S	SHORT
PAD1900	P3V3S_SSD	SHORT

MV_0102

ID PIN FOR BIOS

MV_1225

PROJECT_ID	R42 15W	U22 15W
R4612	MOUNT	OPEN
R4611	OPEN	MOUNT
	3V	0V

BOARD_ID2	M18-70	M18-30
R4617	MOUNT	OPEN
R4618	OPEN	MOUNT
	3V	0V

GPU_PRINTE	UMA	DIS
R4615	MOUNT	OPEN
R4614	OPEN	MOUNT
	3V	0V

GPU_PYWRK	UMA	DIS
	MOUNT	OPEN

BUILD_ID	ID1 00000000	ID0 00000000
DB	0	0
SI	0	1
PV	1	0
MV	1	1

BOARD_ID0	17	14
R4616	MOUNT	OPEN
R4620	OPEN	MOUNT
	3V	0V

BOARD_ID1	VRAMF4	VRAMF2
R4619	MOUNT	OPEN
R4621	OPEN	MOUNT
	3V	0V

WWAN_SKU_ID	WWAN	Non-WWAN
R4622	MOUNT	OPEN
R4623	OPEN	MOUNT
	3V	0V

ID PIN FOR EC

MV_1225

GPU_UMA_SEL	DIS	UMA
R362	MOUNT	OPEN
R363	OPEN	MOUNT
	3V	0V

Phase_ID	SI	DB	PV / MV
R337	10K_short	10K_short	10K_open
R322	10K_open	10K_short	10K_short
	3V	1.5V	0V

GPU_ID	M18-70	M18-30
R390	MOUNT	OPEN
R391	OPEN	MOUNT
	0V	0V

EC_PROJECT_ID	SNAPE17	GRANGER14
R310	10K_short	10K_open
R311	10K_open	10K_short
	3V	0V

ADP_SEL	65W	45W
R307	MOUNT	OPEN
R309	OPEN	MOUNT
	3V	0V

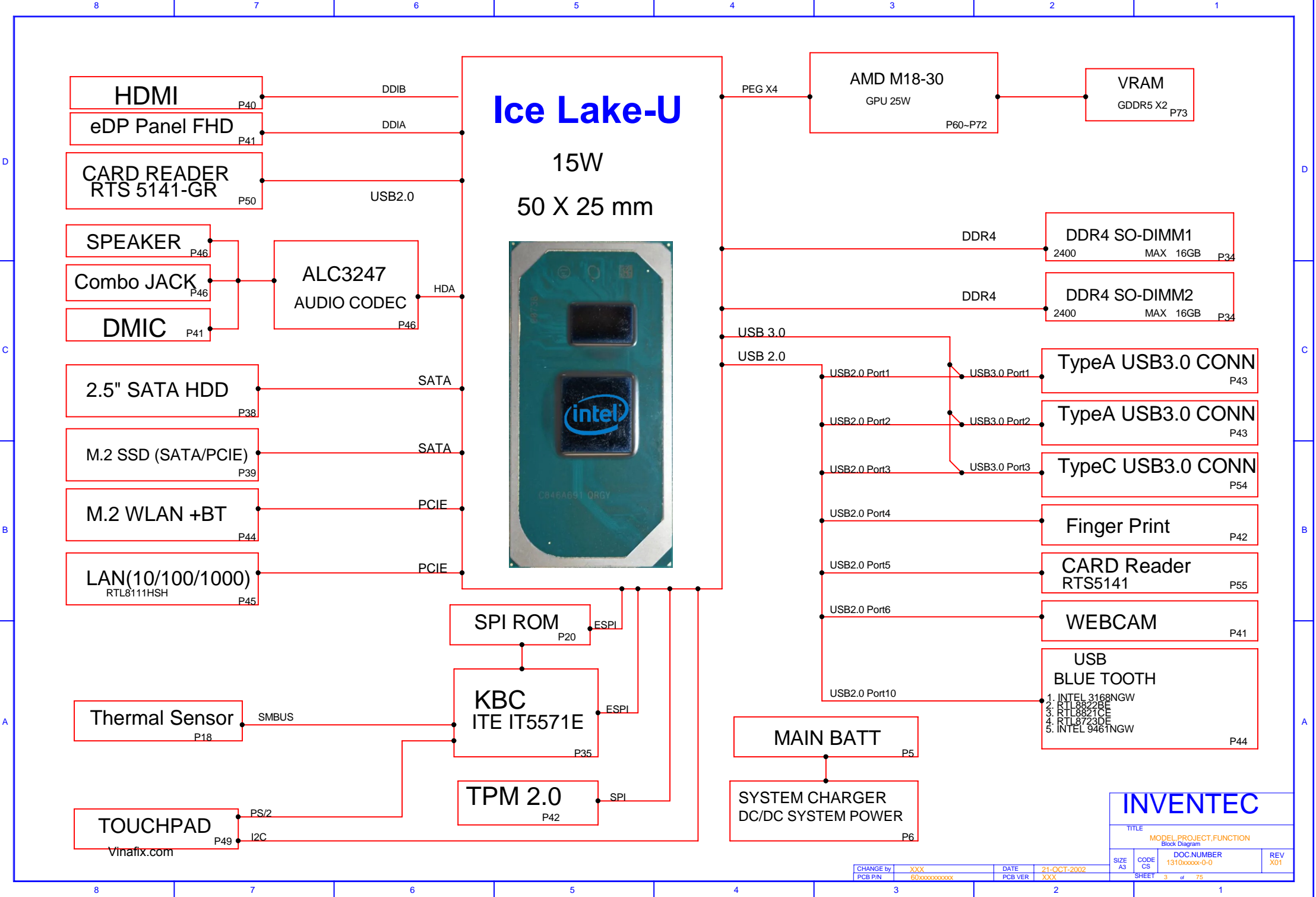
CPU_ID	R42 15W	U22 15W
R343	MOUNT	OPEN
R338	OPEN	MOUNT
	3V	0V

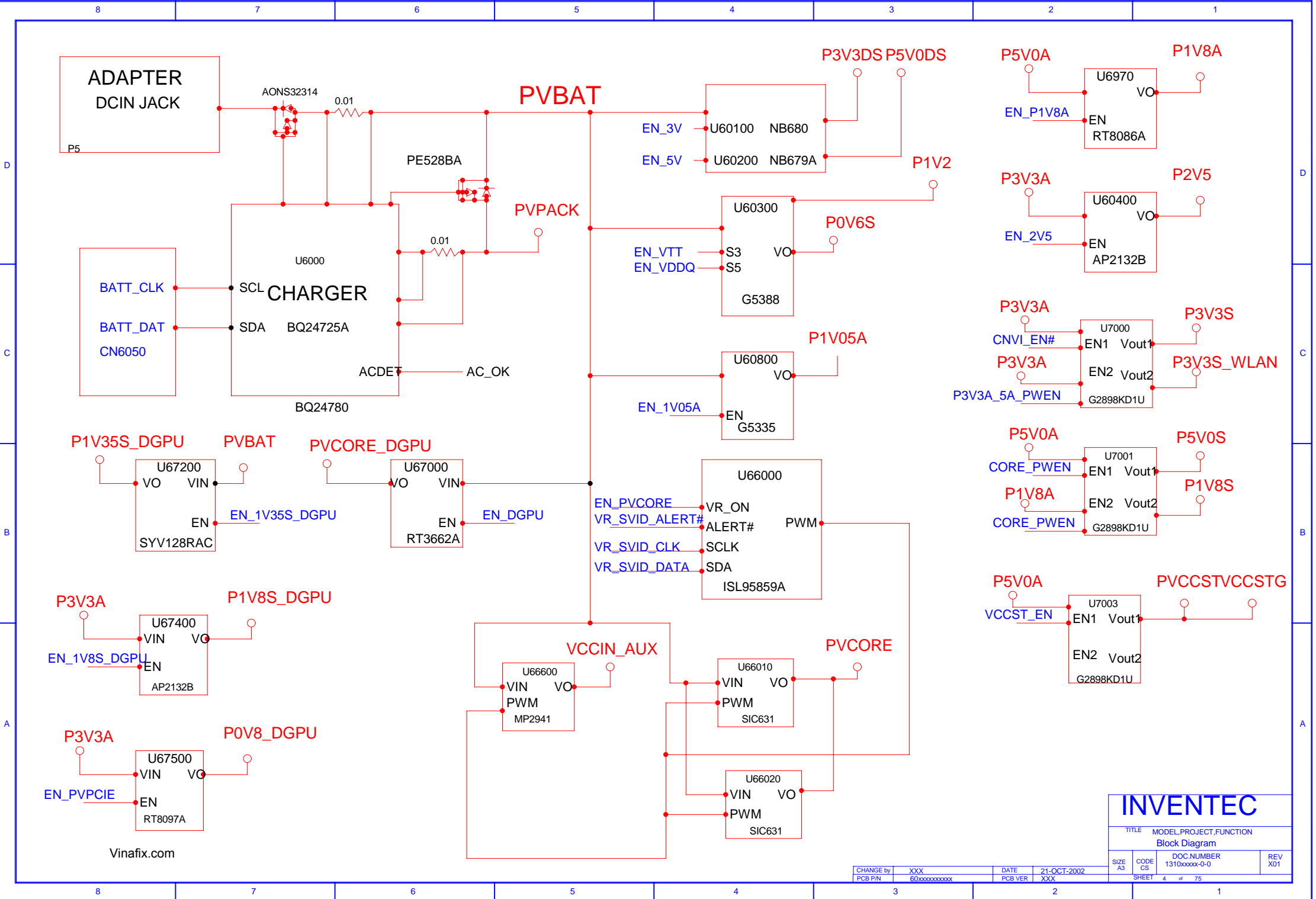
HEDWIG ICL + M18-30 8L	6050A3158801 (8L)
DAUGHTER BOARD (8L)	PICK BUTTON BOARD (TYPE C) 6050A3163901 (8L)
	CARD READER BOARD (TYPE C) 6050A3164201 (8L)

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12 P1V8A_RT8068A
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15 PVCCIN AUX MP2941
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34 CPU STRAP
35 DDR4 DIMM0
36 DDR4 DIMM1

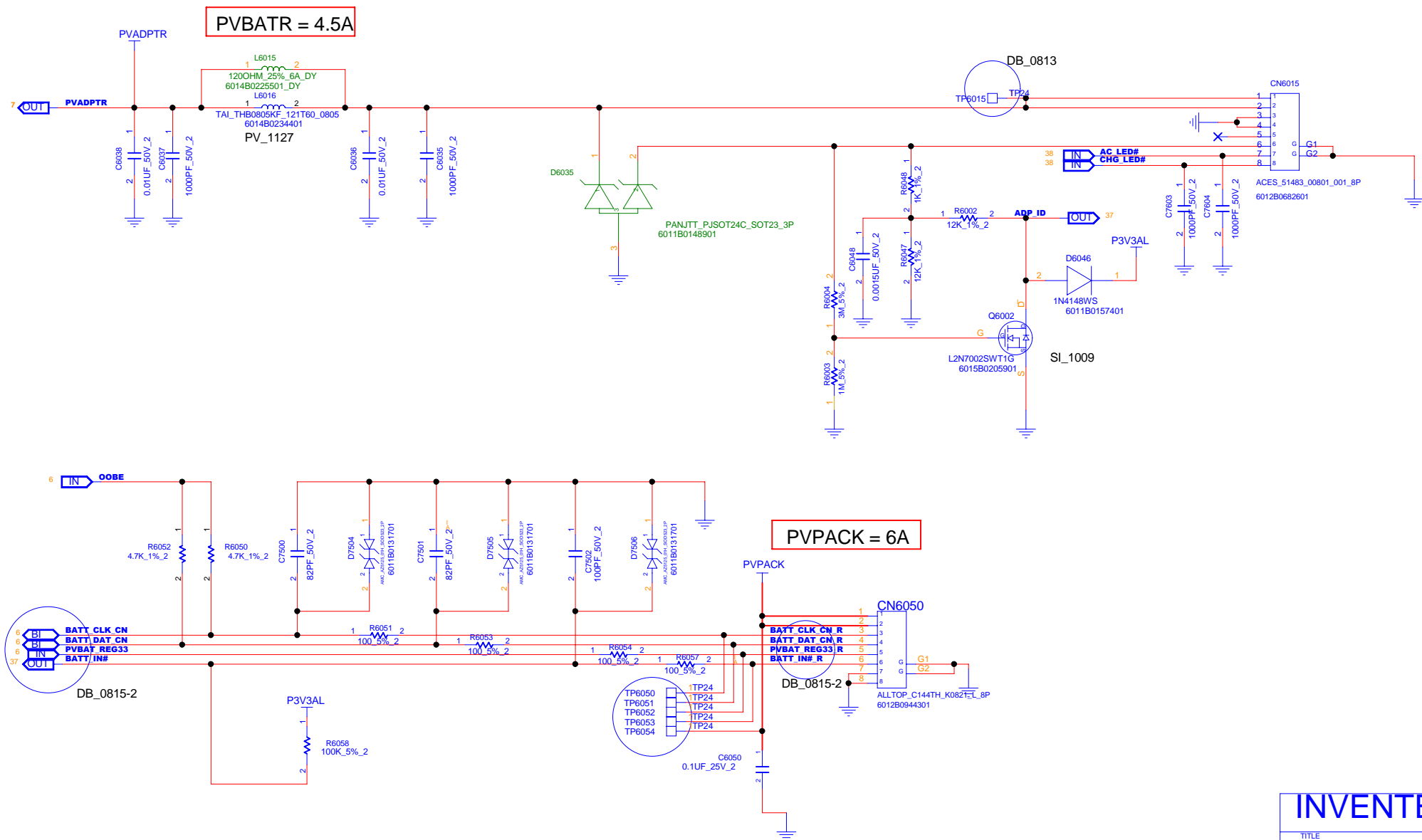
37 EC
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57 DB1-CARD READER
58 DB1-POWER BUTTON & LID
59 DB2-PICK BUTTON
60 GPU COVER
61 PVCORE_DGPU (RT3662A)
62 PVCORE_DGPU MOS
63 P1V35S_DGPU (SYV128RAC)
64 P1V8S_DGPU (AP2132B)
65 P0V8S_DGPU (RT8097A)
66 DGPU POWER SEQUENCE
67 GPU-PCIE
68 GPU-MEMORY
69 GPU-VGA/LVDS/DVI/HDMI/DP
70 GPU-CLOCK/JTAG
71 GPU-THERMAL/DEBUG/GPIO/I2C
72 GPU-POWER/GND
73 VRAM PRO-1
74 VRAM_ID





SELETOR

VER.04_20171113



INVENTEC

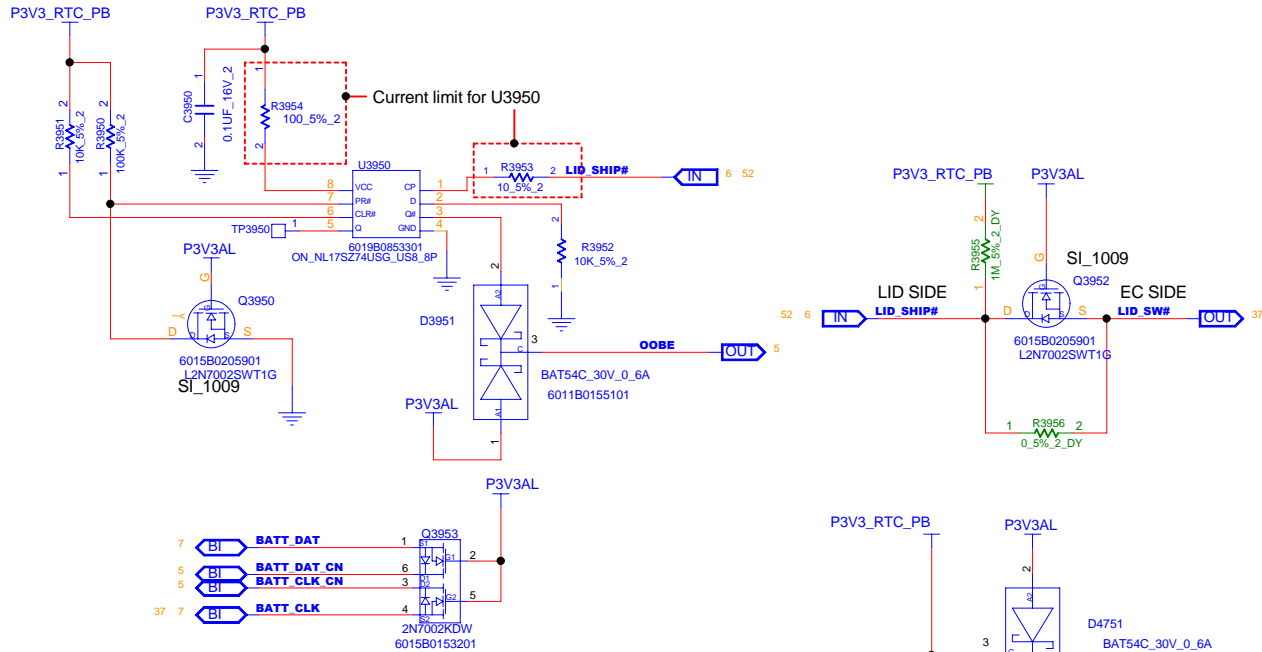
TITLE
MODEL SELECT FUNCTION

SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
SHEET 5 of 75			

CHANGE by PCB P/N	XXX 60xxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
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STORAGE MODE

VER.01_20170918



TRUTH TABLE

INPUT				OUTPUT		OPARATING MODE
PR#	CLR#	CP	D	Q	Q#	
L	H	X	X	L	L	ASYNCHRONOUS SET ASYNCHRONOUS CLEAR UNDETERNLNED
H	L	X	X	L	H	
L	L	X	X	H	H	
H	H	↑	L	L	L	LOAD AND READ REGISTER
H	H	↑	L	L	H	

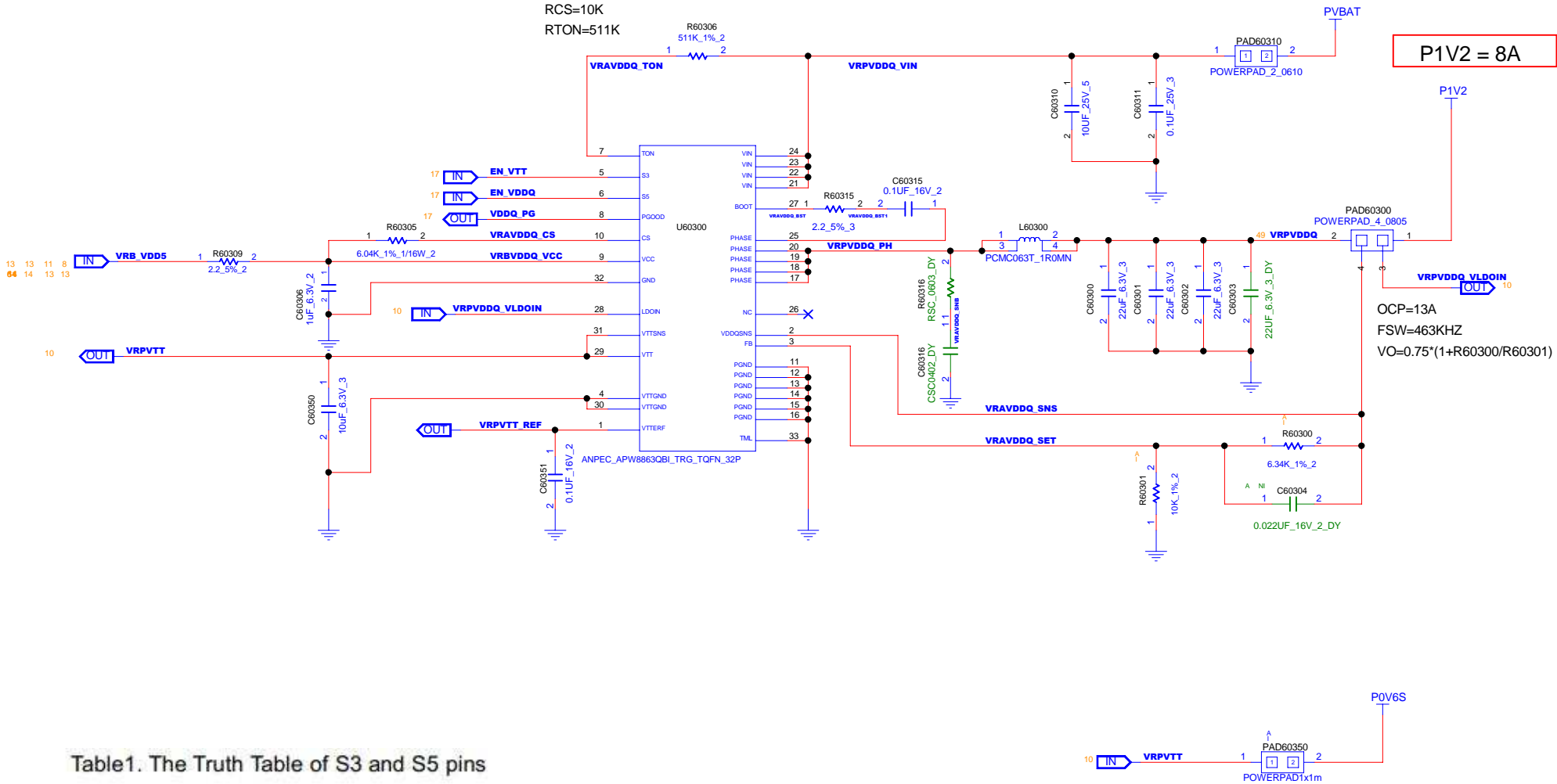
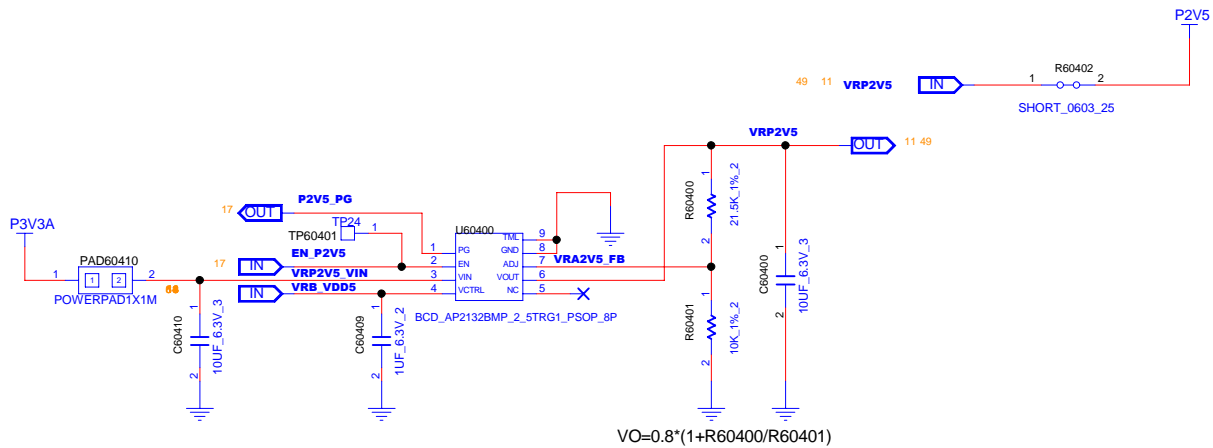
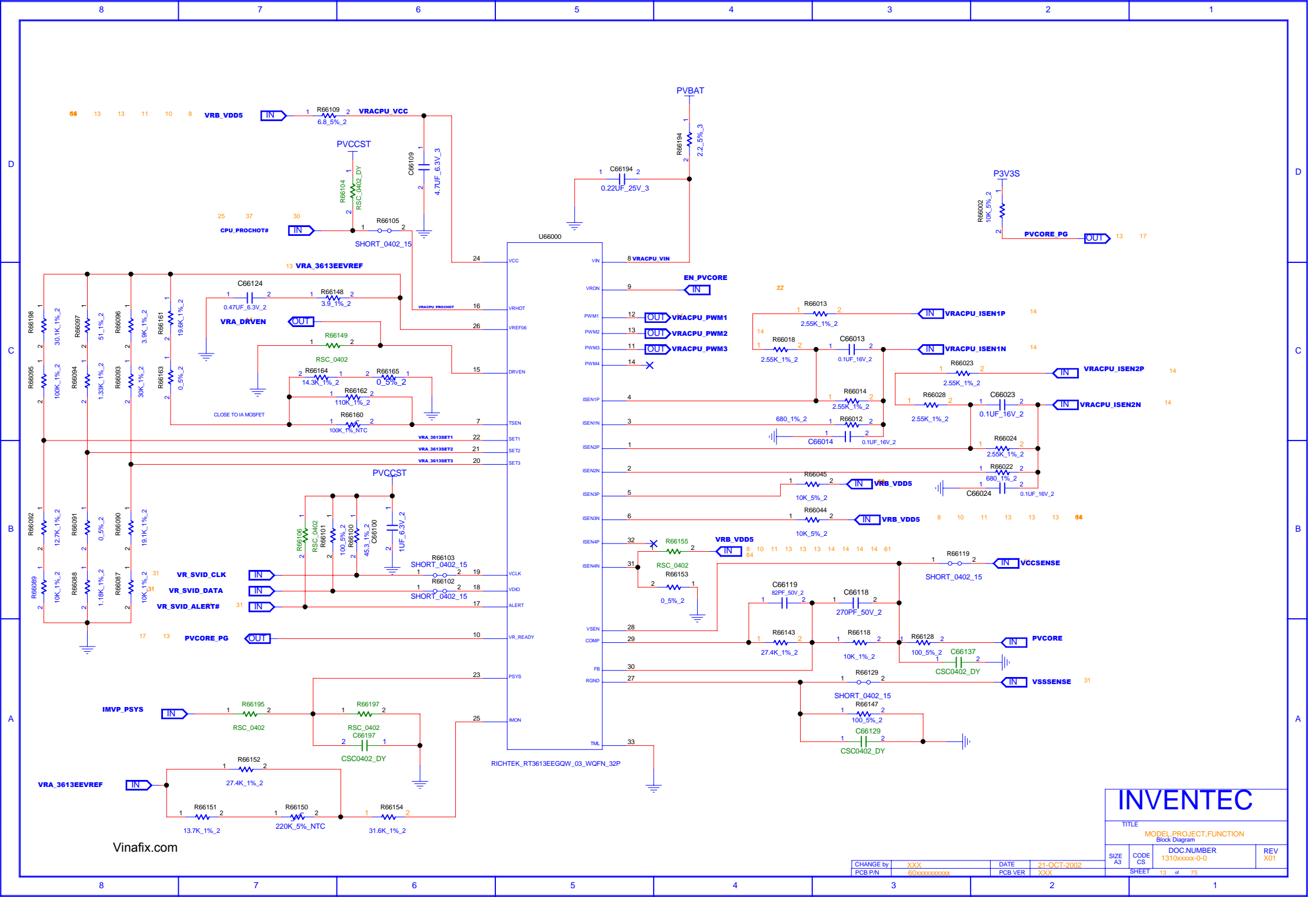
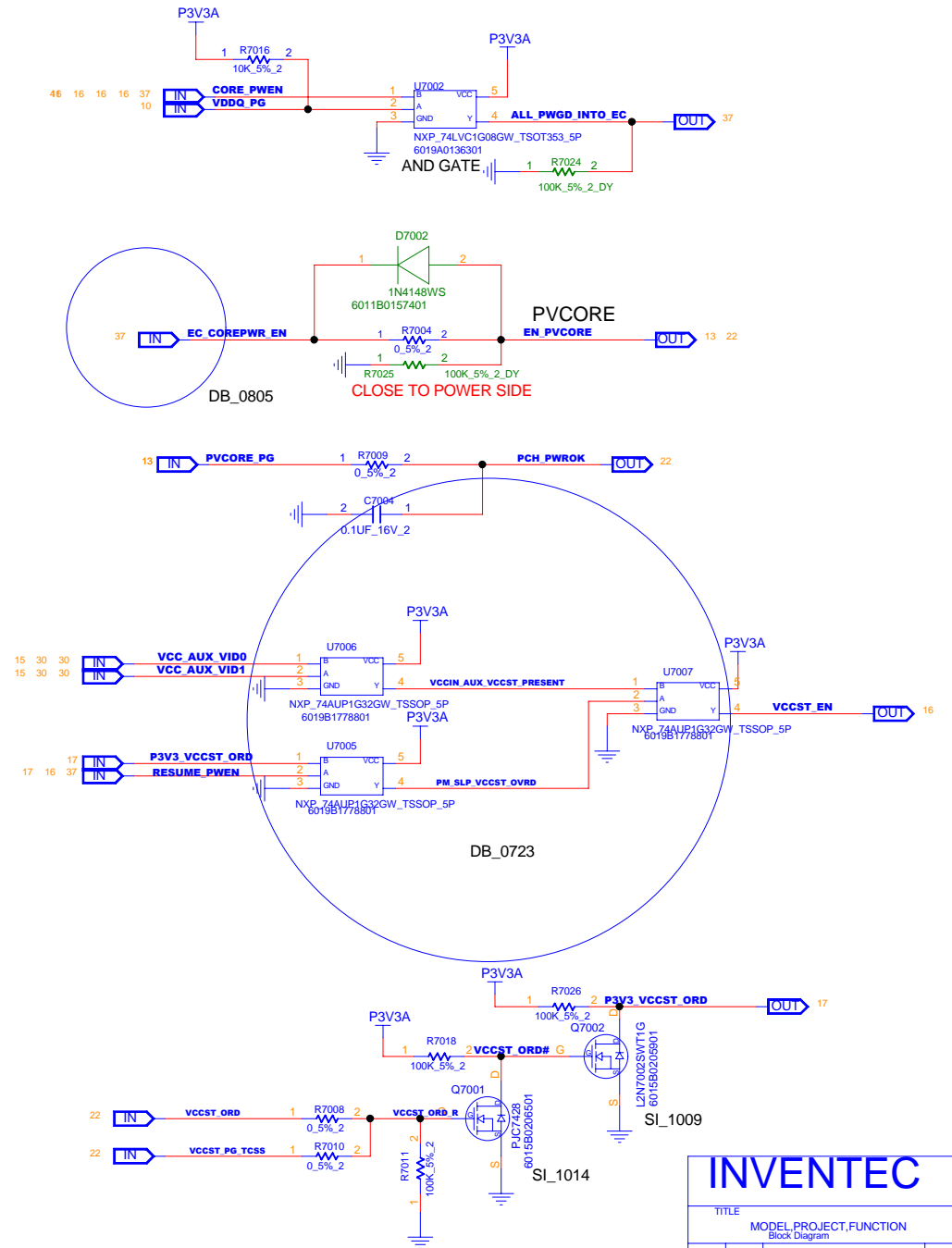
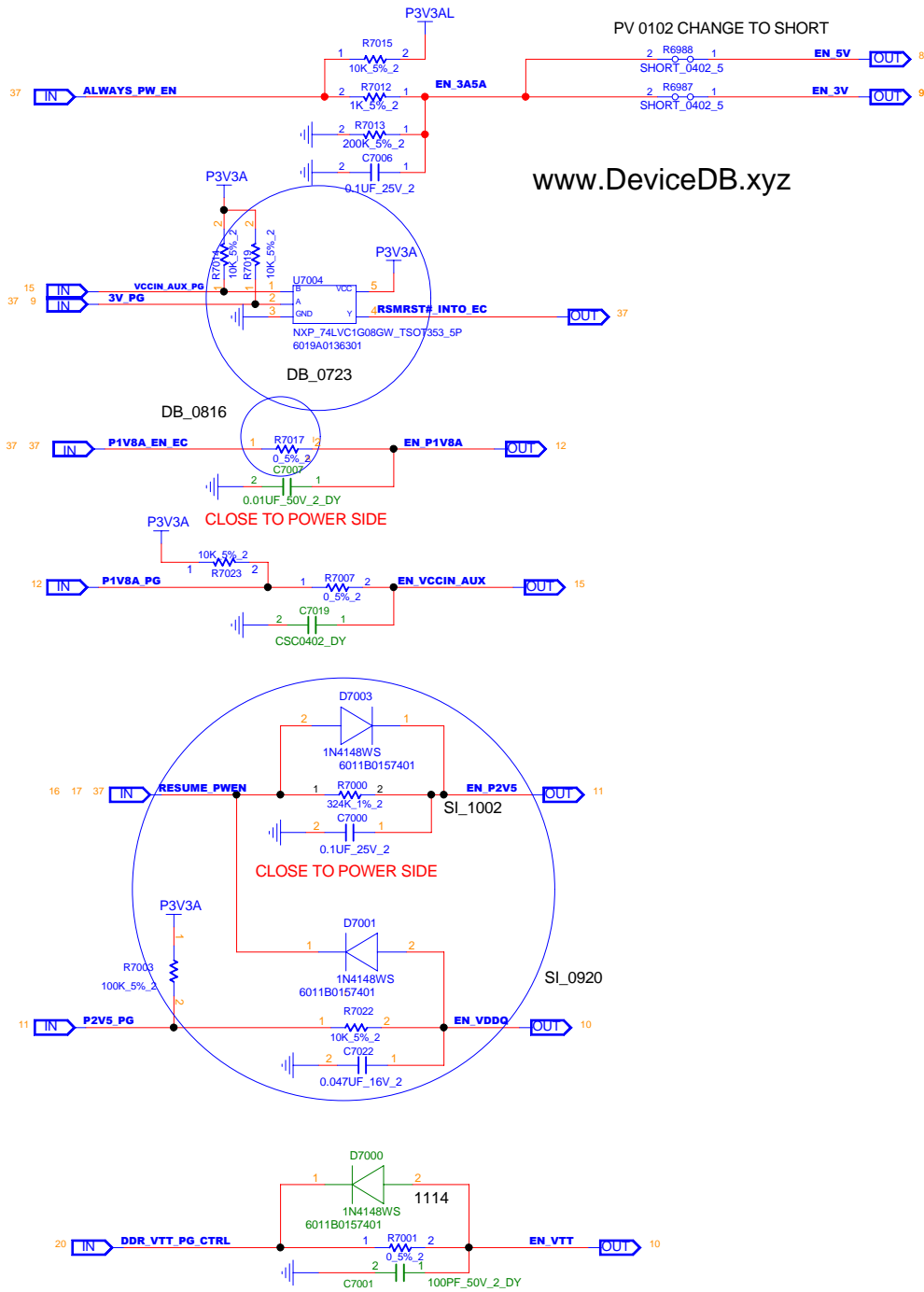


Table1. The Truth Table of S3 and S5 pins

STATE	S3	S5	VDDQ	VTTREF	VTT
S0	H	H	1	1	1
S3	L	H	1	1	0 (high-Z)
S4/5	L	L	0 (discharge)	0 (discharge)	0 (discharge)







INVENTEC

TITLE
MODEL PROJECT FUNCTION
Block Diagram

SIZE A3 CODE CS DOC NUMBER 1310xxxx-0-0 REV X01

CHANGE by XXX DATE PCB VER 2002

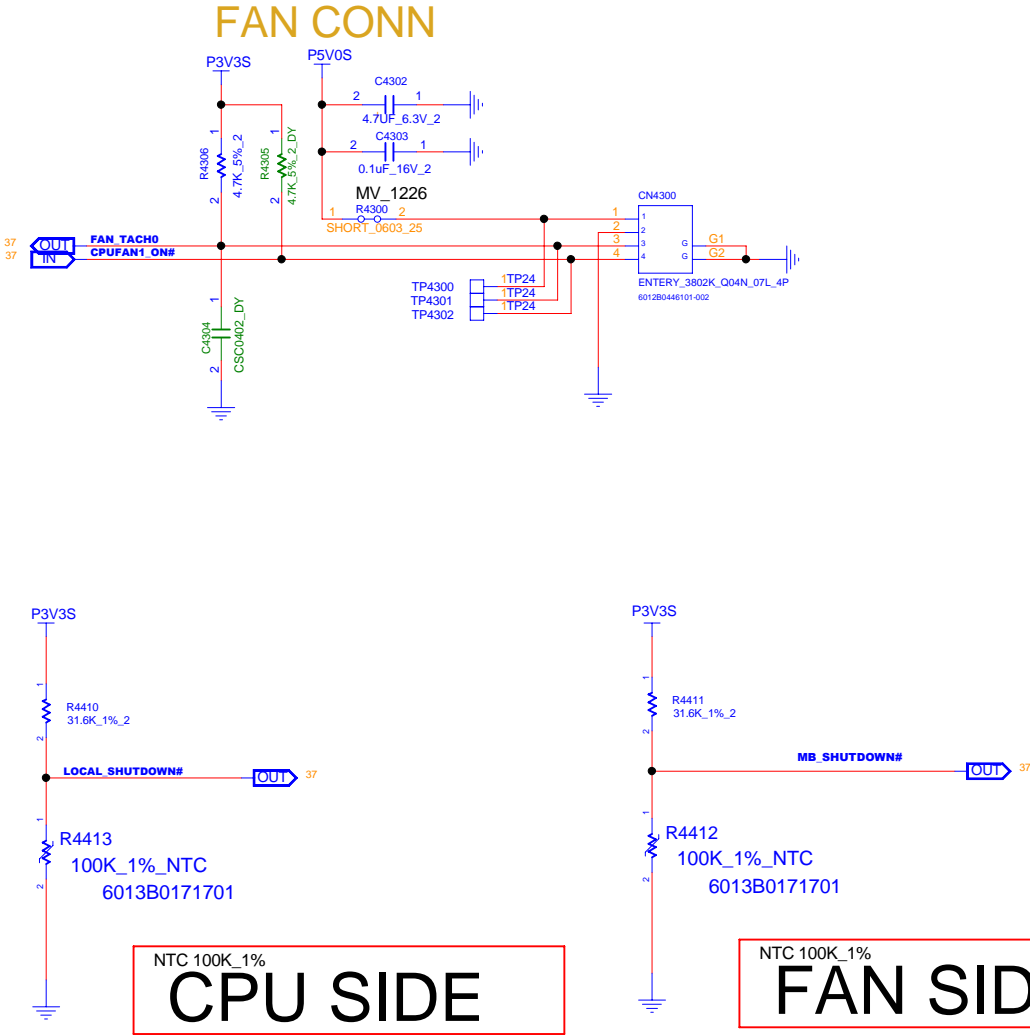
SHEET 17 75



FAN & THERMAL

FOR BIG CORE USE

VER.04_20171011



INVENTEC

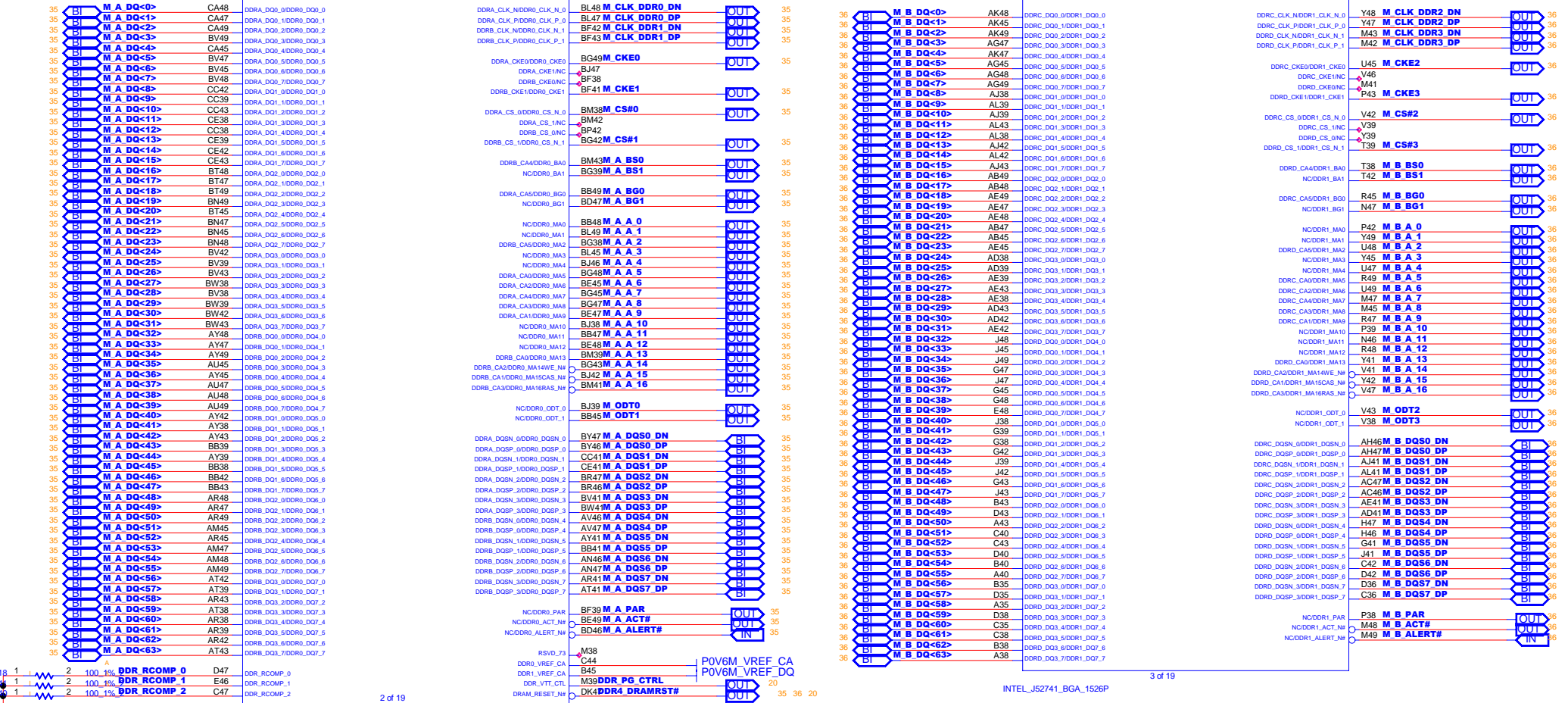
TITLE
MODEL PROJECT FUNCTION
THERMAL & FAN

SIZE A3 CODE CS DOC NUMBER 1310xxxx-0-0 REV X01

SHEET 19 of 75

U4555

U4555



REFERENCE:4500~4949

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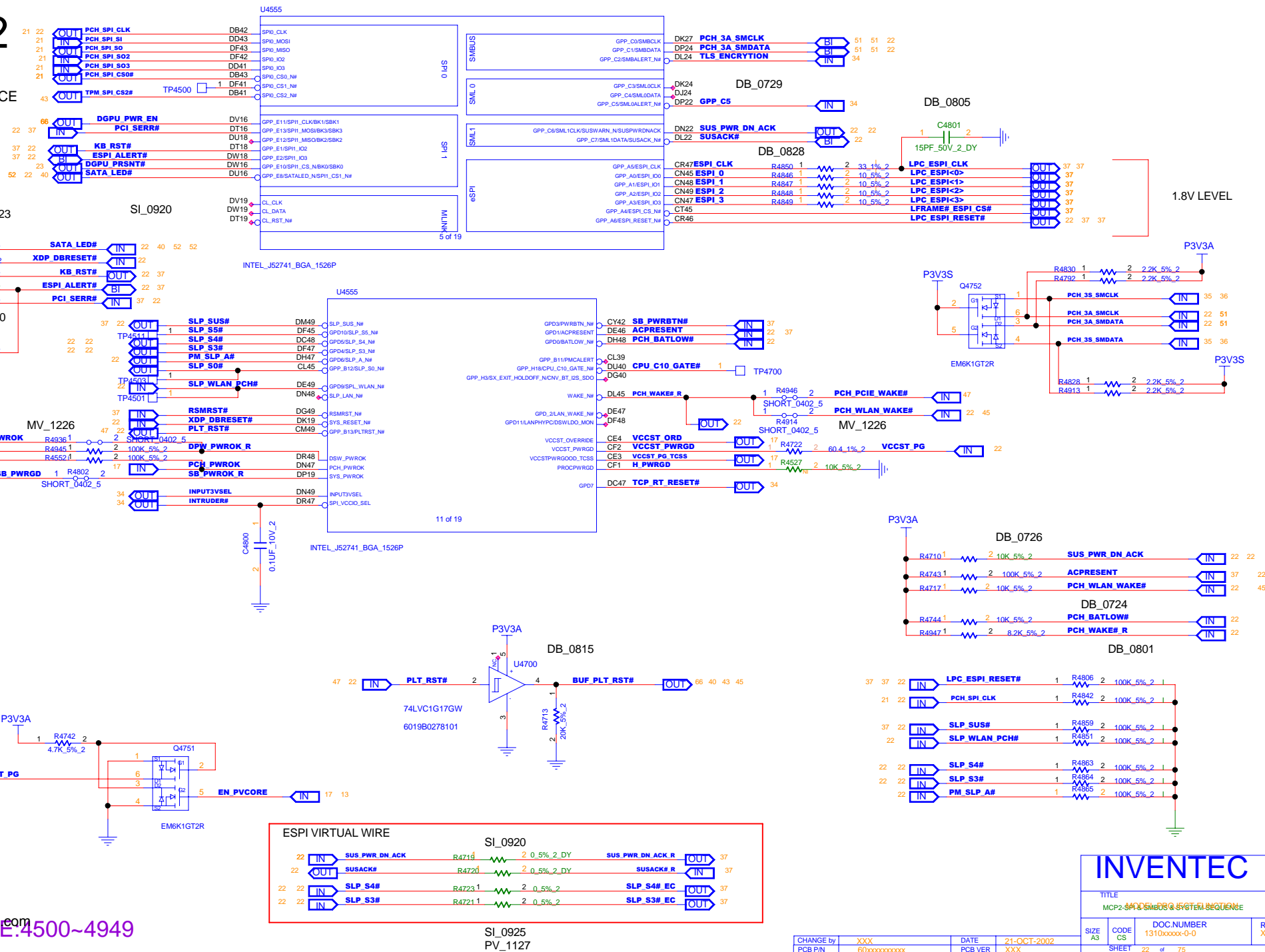
INVENTEC

TITLE MODEL PROJECT FUNCTION
MCPS-DDRSIZE CODE CS DOC NUMBER REV
A3 CS 1310xxxx-0-0 X01CHANGE by XXX DATE 21-OCT-2002
PCB P/N 60xxxxxxxxx PCB VER XXX

SHEET 20 of 75

CPU-2

SPI
SMBUS
SYSTEM SEQUENCE



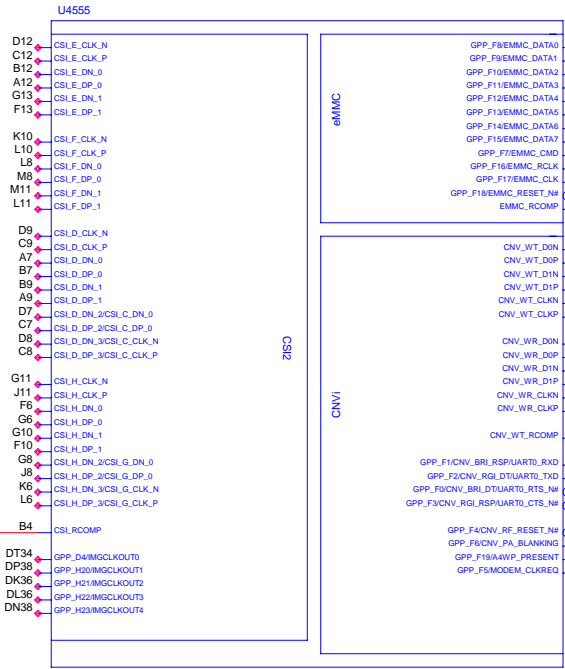
REFERENCE:4500~4949

CPU-4 GPIO, CNVI

DB_0726

DB_0815-2

DB_0814



INTEL_J52741_BGA_1526P

9 of 19

DB_0815-2

SI_0910

SI_0918

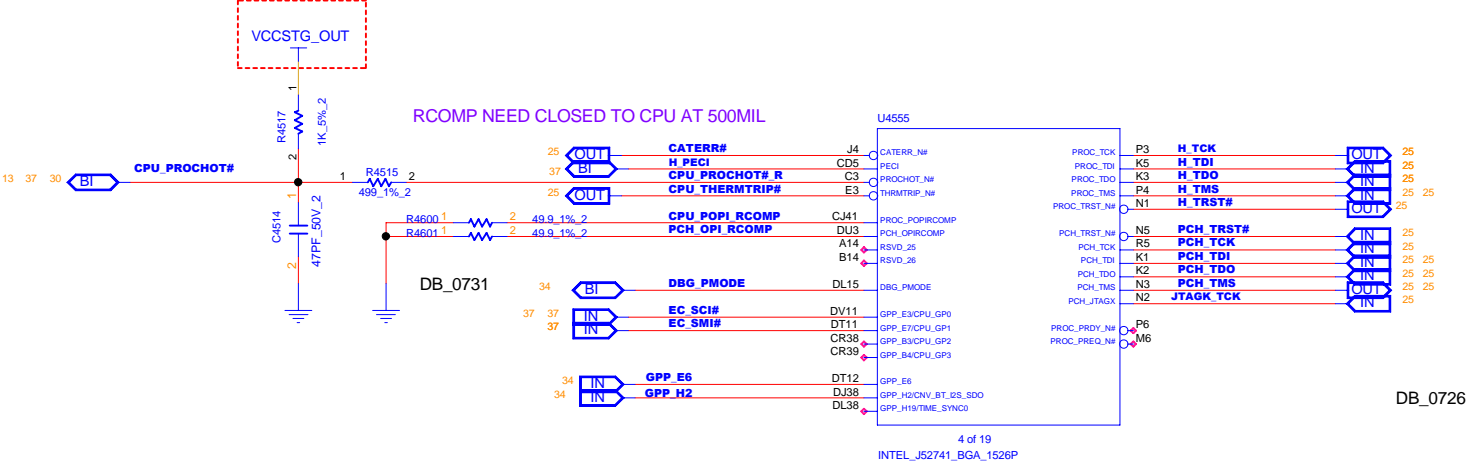
INVENTEC

REFERENCE:4500~4949
Vinafix.com

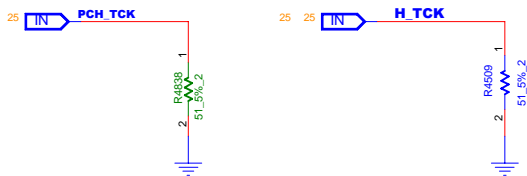
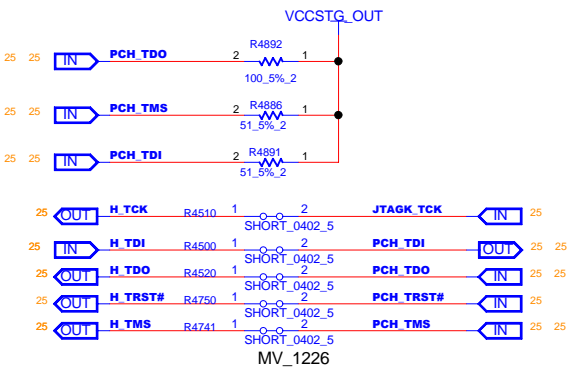
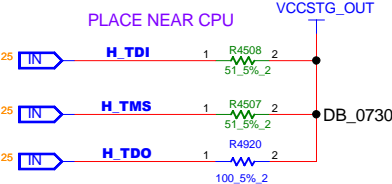
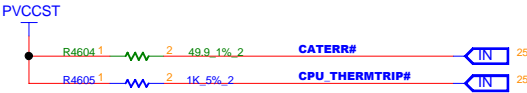
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

TITLE			
MODEL PROJECT FUNCTION			
MCP4-GPIO & CNVI			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET 24 of 75			

CPU-5 MISC



PINS A14 & B14 ARE USED IN U43E PACKAGE, ADD RCOMP RESISTORS FOR U43E COMPATIBLE DESIGNS



REFERENCE: 4500~4949

INVENTEC

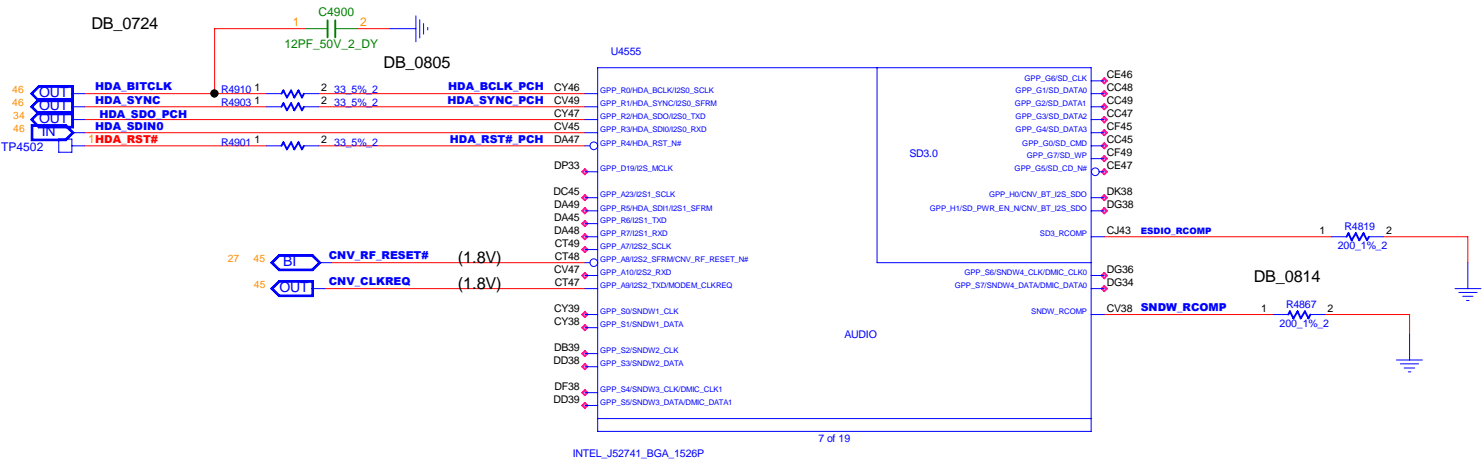
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SIZE A3 CODE CS DOC NUMBER 1310xxxx-0-0 REV X01

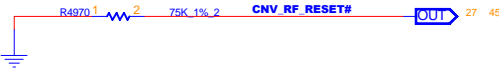
CHANGE by XXX DATE 21-OCT-2002 PCB P/N 60xxxxxxxxx PCB VER XXX

SHEET 25 of 75

CPU-7 RTC, AUDIO, SATA



LAYOUT NOTE: PLACE R4808 NEAR PCH
LAYOUT NOTE: JTAG_TMS TERMINATIONS NEED TO BE PLACED NEAR PCH
LAYOUT NOTE: JTAG_TDI TERMINATIONS NEED TO BE PLACED NEAR PCH
LAYOUT NOTE: JTAG_TDO TERMINATIONS NEED TO BE PLACED NEAR XDP



REFERENCE:4500~4949
Vinafix.com

INVENTEC

TITLE
MODEL PROJECT FUNCTION
MC77-RTC & AUDIO & SATA

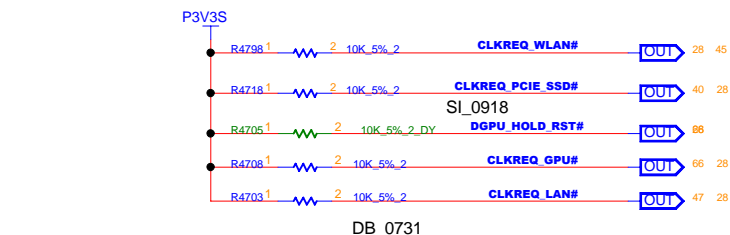
SIZE A3
CODE CS
DOC NUMBER 1310xxxx-0-0
REV X01
SHEET 27 of 75

CHANGE by XXX
PCB P/N 60xxxxxxxxx
DATE 21-OCT-2002
PCB VER XXX

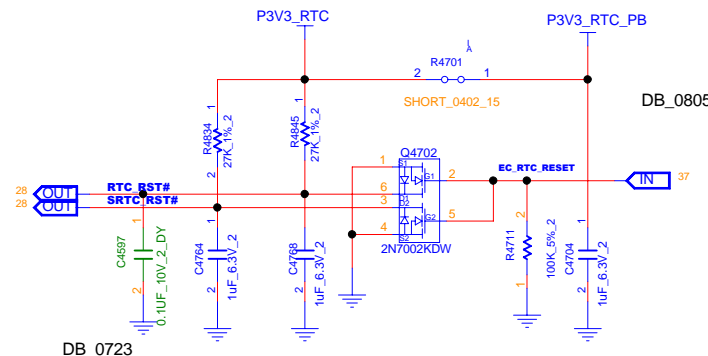
CPU-8

CLOCK, RESERVED

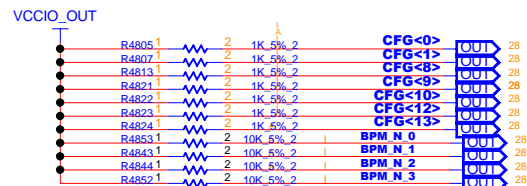
RTC



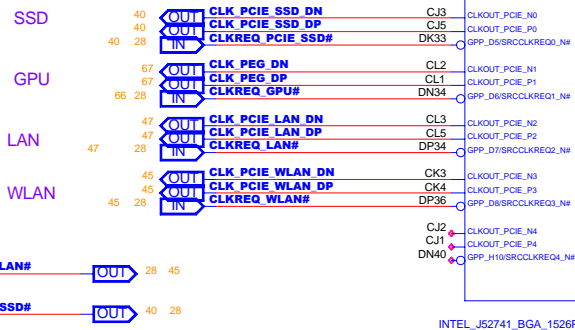
DB_0731



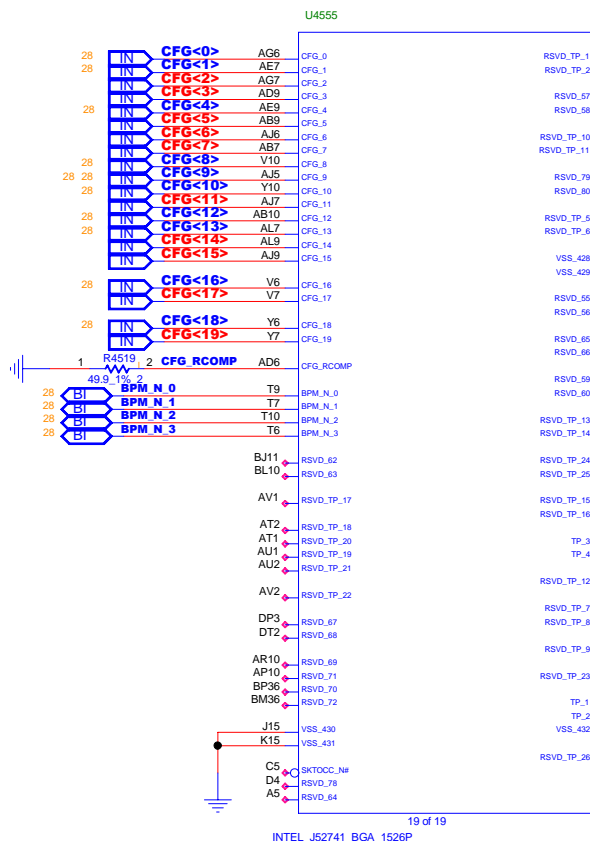
DB_0723



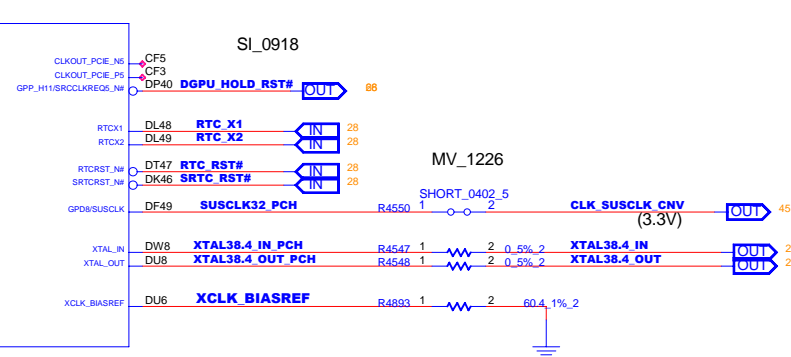
Vinafix.com
REFERENCE:4500~4949



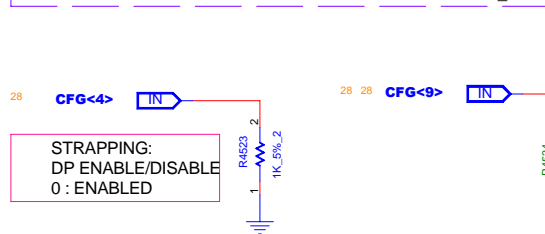
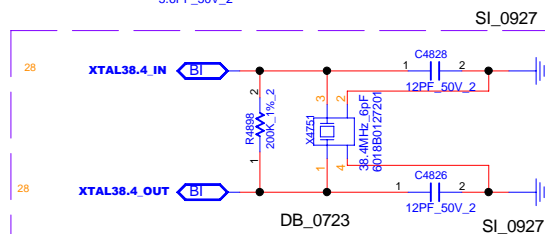
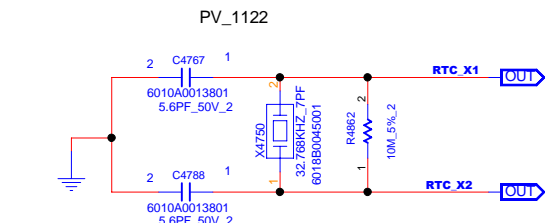
INTEL_J52741_BGA_1526P



INTEL_J52741_BGA_1526P



INTEL_J52741_BGA_1526P



INVENTEC			
TITLE			
MODEL PROJECT FUNCTION			
MCPE-CLOCK & RESERVED			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET 28 of 75			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxx	PCB VER	XXX

CPU-12 POWER2

ROUTE VCCSENSE WITH 27.4OHM IMPEDANCE

PLACE IN BACK SIDE

PLACE IN BACK SIDE

PLACE IN TOP SIDE

PLEASE PLACE CAPS CLOSE TO CPU

Table 11-8. Differences between Power Maps

Volume	Premium
VccSTG gated by SLP_S3#	VccSTG gated by {CPU_C10_GATE#}
VccPLL_OC is supplied directly from VDDQ	VccPLL_OC is supplied from VDDQ through a load switch
VCC1P8A on the CPU is supplied directly by V1.8A	VCC1P8A is supplied from V1.8A and gated by CPU_C10_GATE #
VCC_VNNEXT_1P05 is not used	VCC_VNNEXT_1P05 is supplied by small dedicated VNN VR to bypass PCH FIVR during light load
VCC_V1P05EXT_1P05 is not used	VCC_V1P05EXT_1P05 is supplied by small dedicated V1.05A VR to bypass PCH FIVR during light load

REFERENCE:4500~4949

INVENTEC

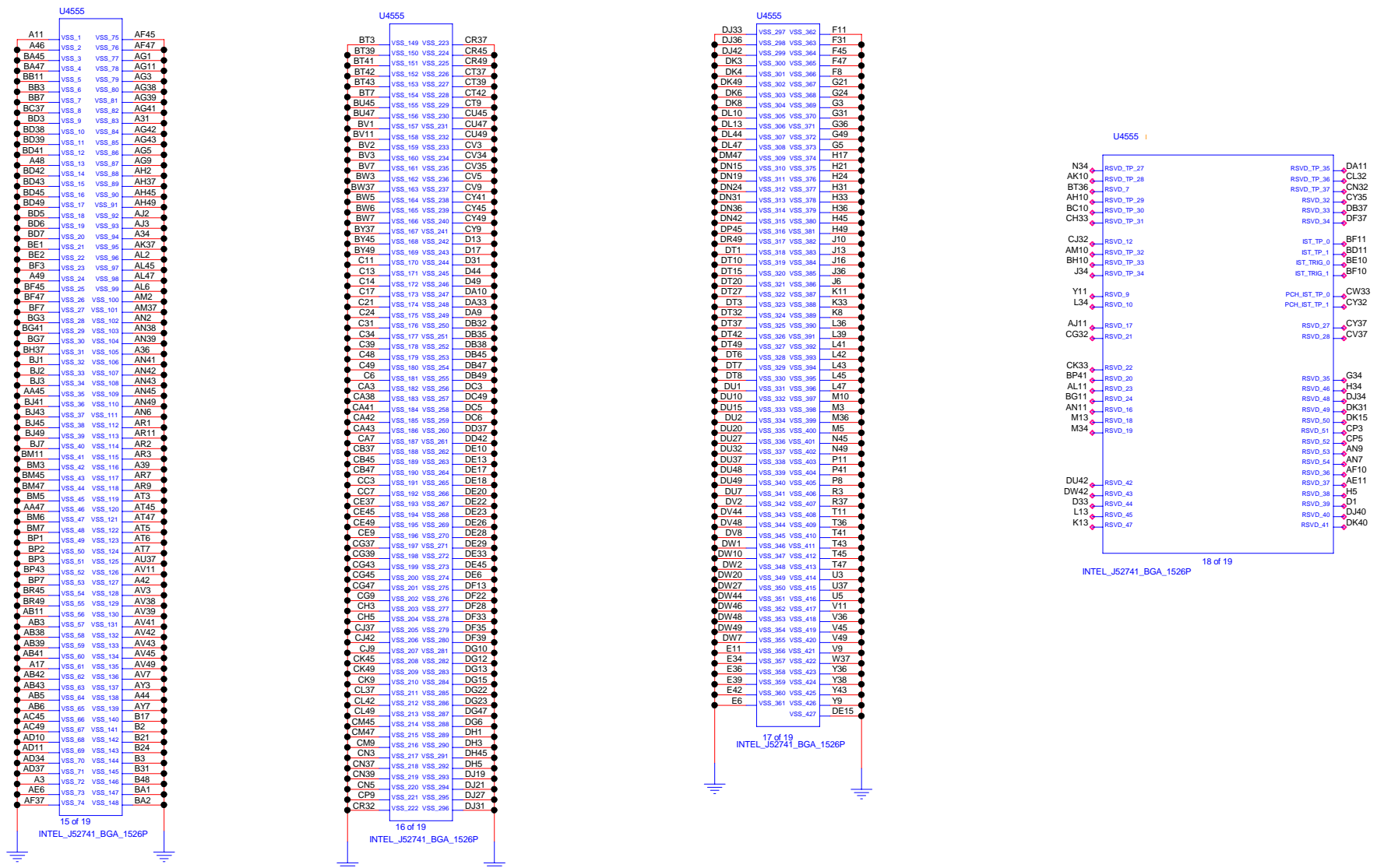
TITLE
MONITOR POWER FUNCTION

SIZE A3 CODE CS DOC NUMBER 1310xxxx-0-0 REV X01

CHANGE by XXX DATE 21-OCT-2002
PCB P/N 60xxxxxxxxx PCB VER XXX

SHEET 32 of 75

CPU-13 GND



REFERENCE:4500~4949

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INVENTEC

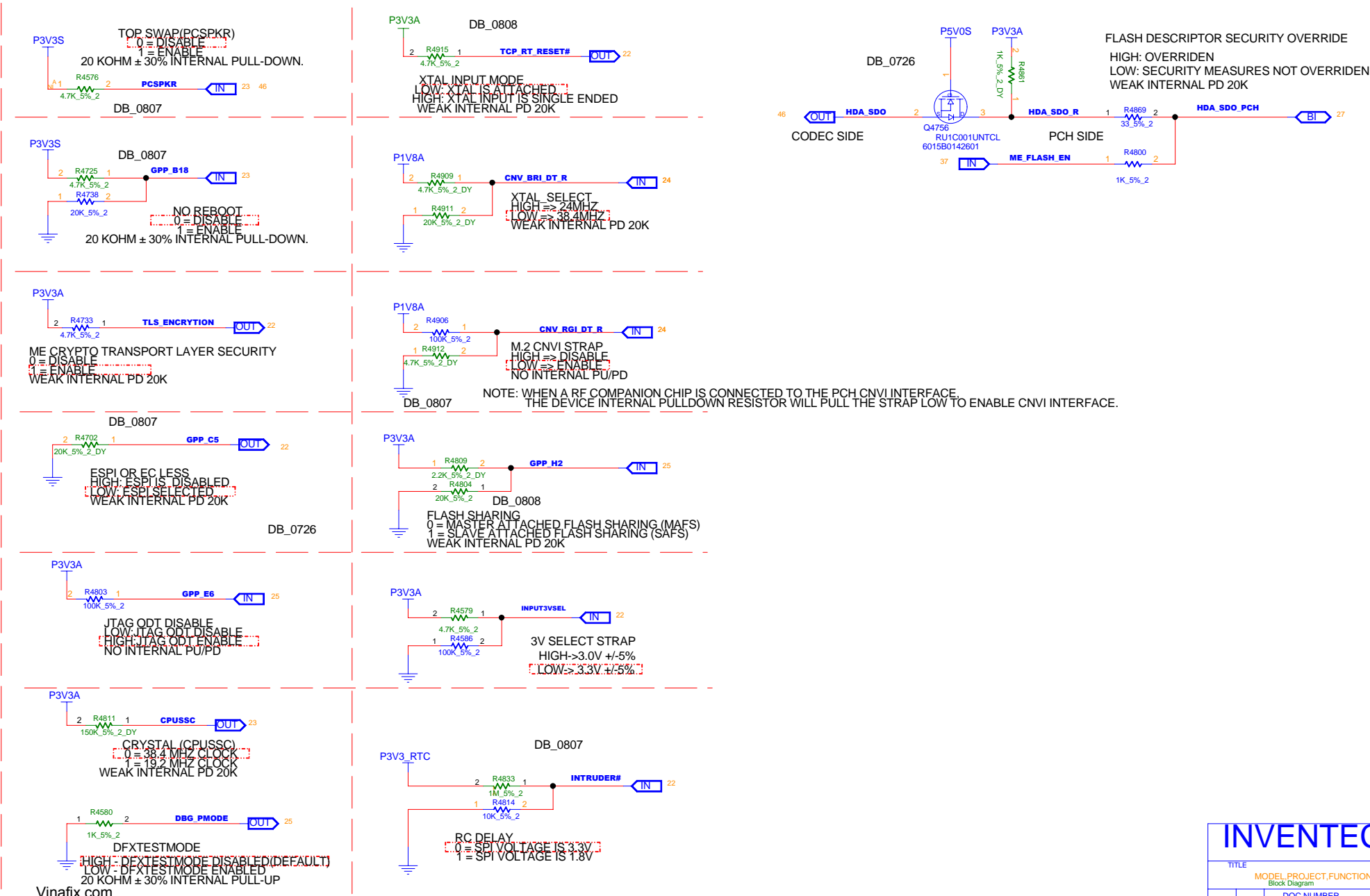
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MODEL PROJECT FUNCTION

SIZE A3 CODE CS DOC NUMBER 1310xxxx-0-0 REV X01

CHANGE by XXX DATE 21-OCT-2002
PCB P/N 60xxxxxxxxx PCB VER XXX

SHEET 33 of 75

CPU-14 STRAP



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INVENTEC

TITLE
MODEL PROJECT FUNCTION
Block Diagram

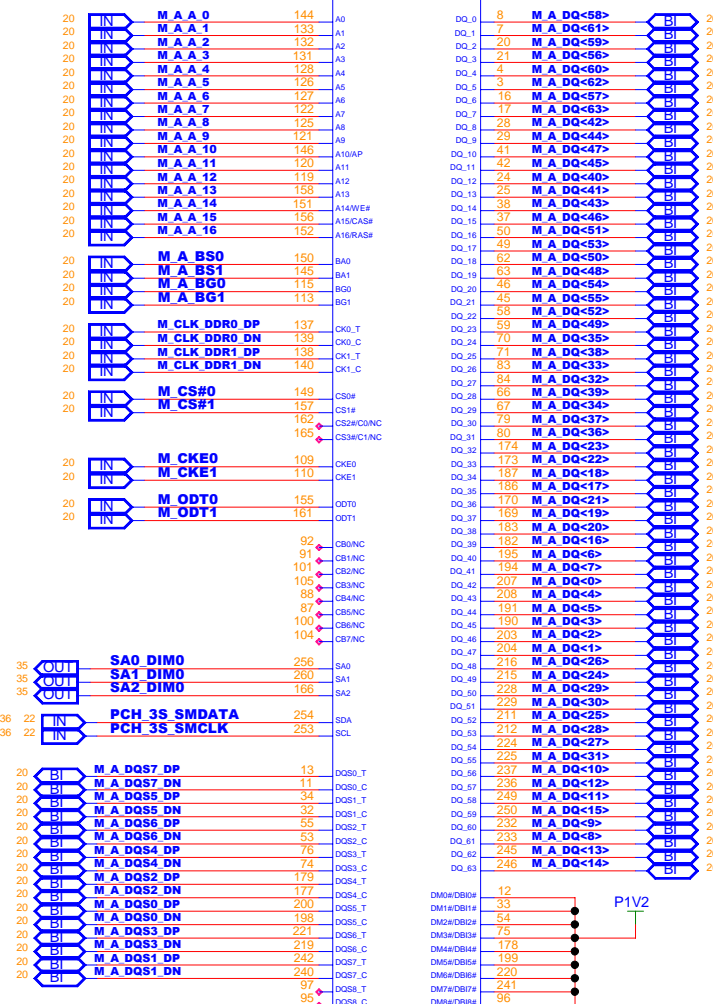
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
SHEET 34 of 75			

CHANGE by PCB P/N	XXX 60xxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
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REFERENCE 4100~4299(DDR)

CHA
H=4

CN4200



ARGOSY_D4AR0_26010_1P40_260P
6026B0328101-004

SPD ADDRESS FOR CHANNEL-0
WRITE ADDRESS:0XA0

RED ADDRESS :0XA1

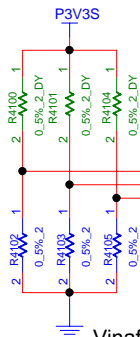
SA0=0,SA1=0,SA2=0

DDR4 FOR OPERATING SPEED:1867 MT/S

STRETCH GOAL IS 2133 MT/S

EVENT_N: INDICATES THERMAL EVENT ON DIMM.

EVENT_N:ON ECC DIMM:KEEP A PULL UP IF NO PIN IN PCH

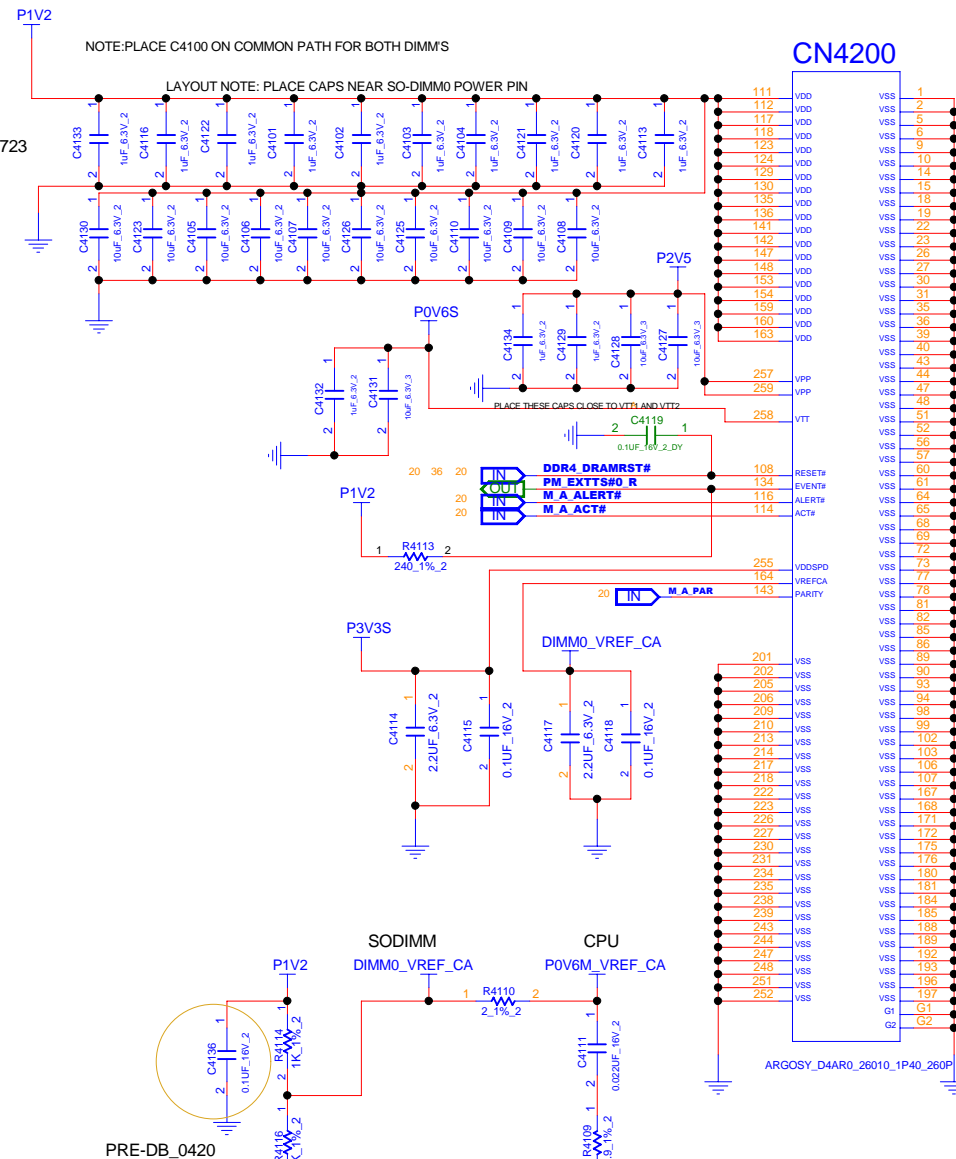


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NOTE:PLACE C4100 ON COMMON PATH FOR BOTH DIMM'S

LAYOUT NOTE: PLACE CAPS NEAR SO-DIMMO POWER PIN

DB_0723



PRE-DB_0420

CN4200

INVENTEC

TITLE
MODEL PROJECT FUNCTION

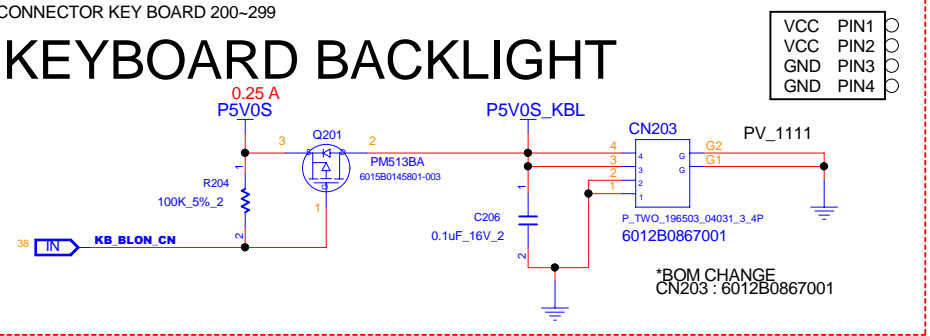
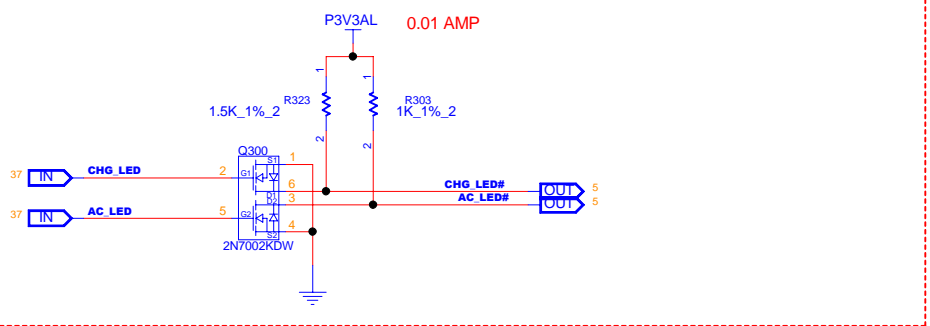
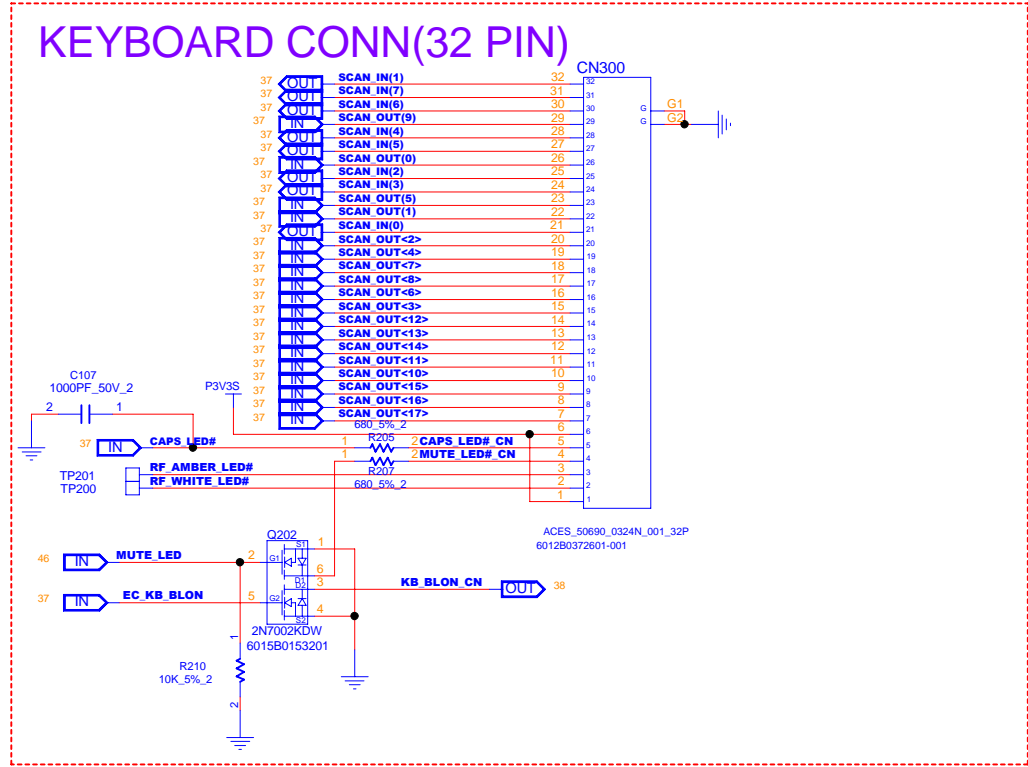
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET	35	of 75	

CHANGE by	DATE
XXX	21-OCT-2002
PCB P/N	PCB VER
60xxxxxxxxxx	XXX

KEYBOARD CONNECTOR

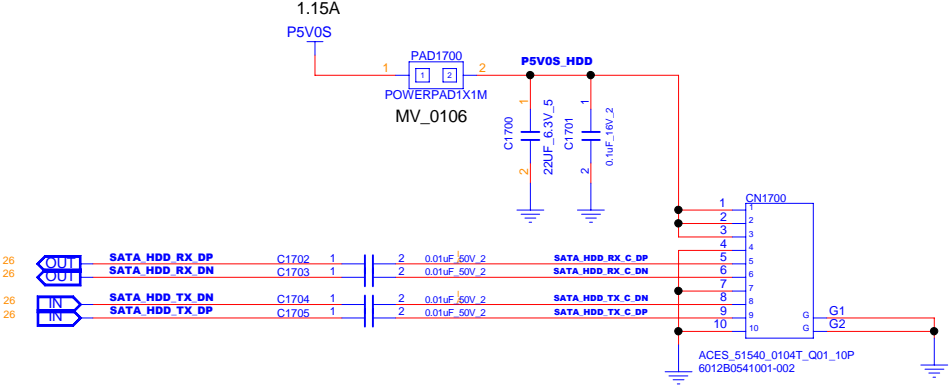
VER.07_20171110

KEYBOARD CONN(32 PIN)



SATA HDD CABLE CONN on MB

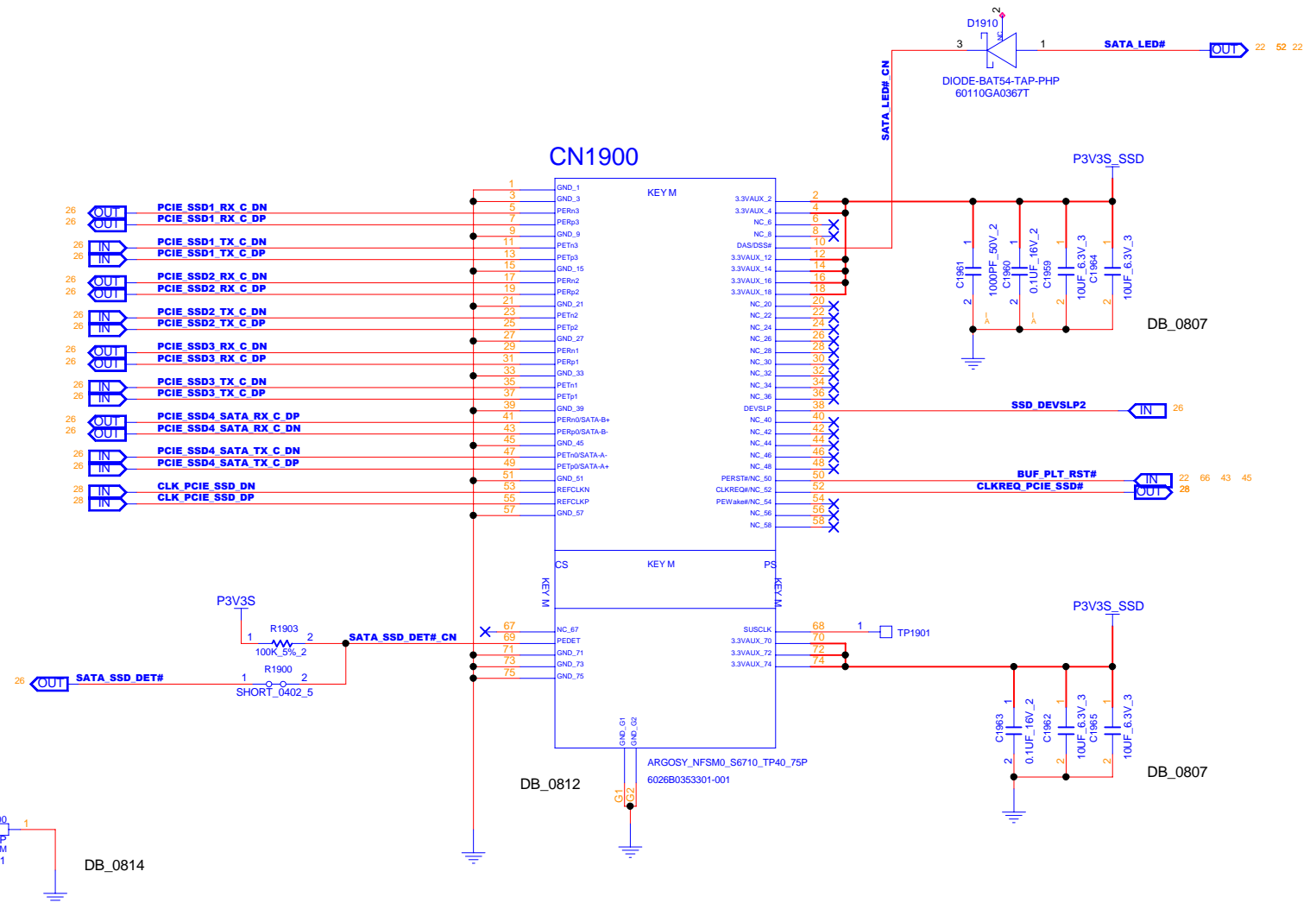
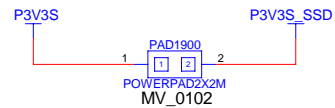
VER.01_20170918



M.2 SSD

REFERENCE NUMBER:1900~1949

VER.03_20171004



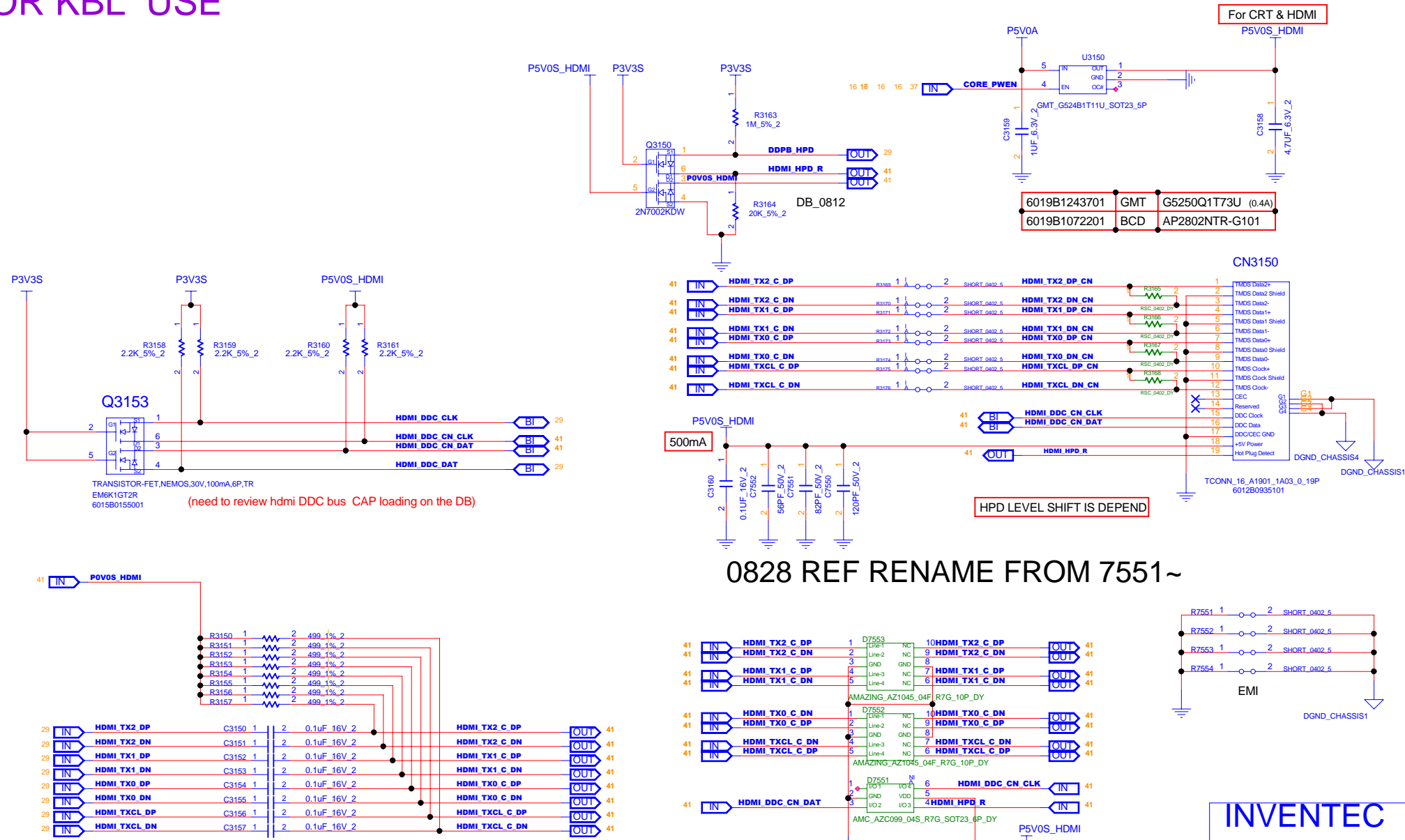
INVENTEC				
TITLE				
MODEL PROJECT,FUNCTION NGFF- SSD				
SIZE	CODE	DOC NUMBER	REV	
A3	CS	1310xxxx-0-0	X01	
SHEET of 40 75				

HDMI

Location 3150 ~ 3199

VER.08_20171115-2

FOR KBL USE



0828 REF RENAME FROM 7551~

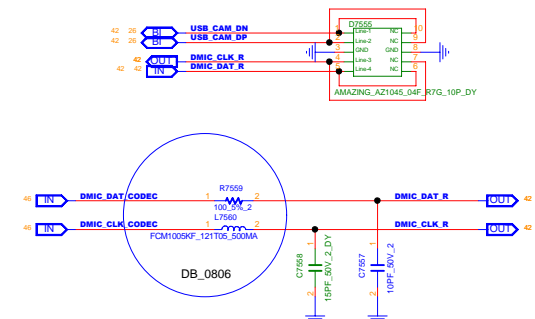
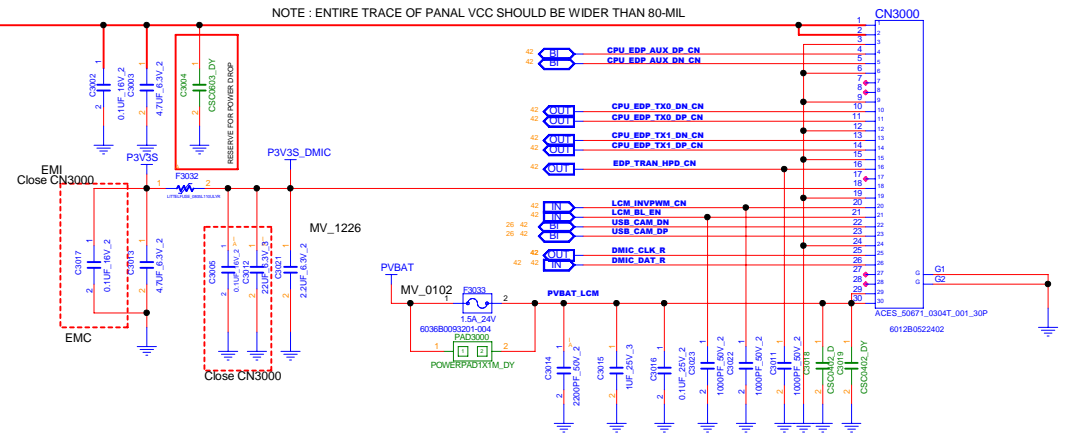
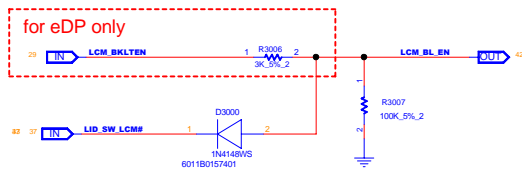
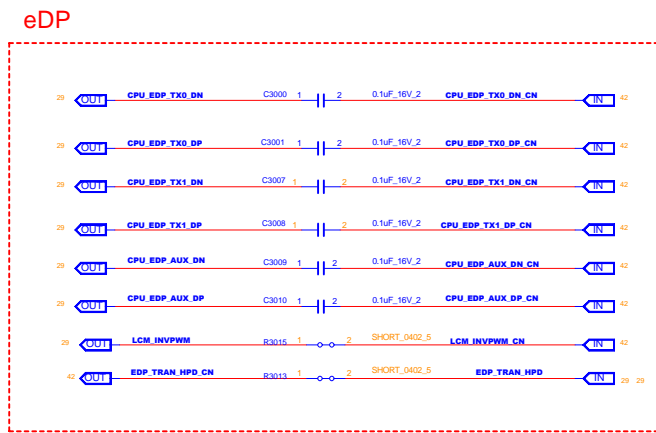
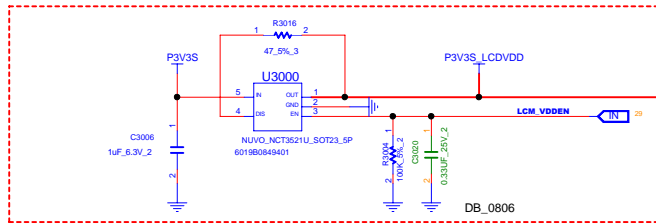
INVENTEC

TITLE			
MODEL PROJECT FUNCTION			
HDMI CORN			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET 41 of 75			

CHANGE by	XENG	DATE	21-OCT-2002
PCB P/N	60xxxxxxx	PCB VER	XVER

LCM : eDP

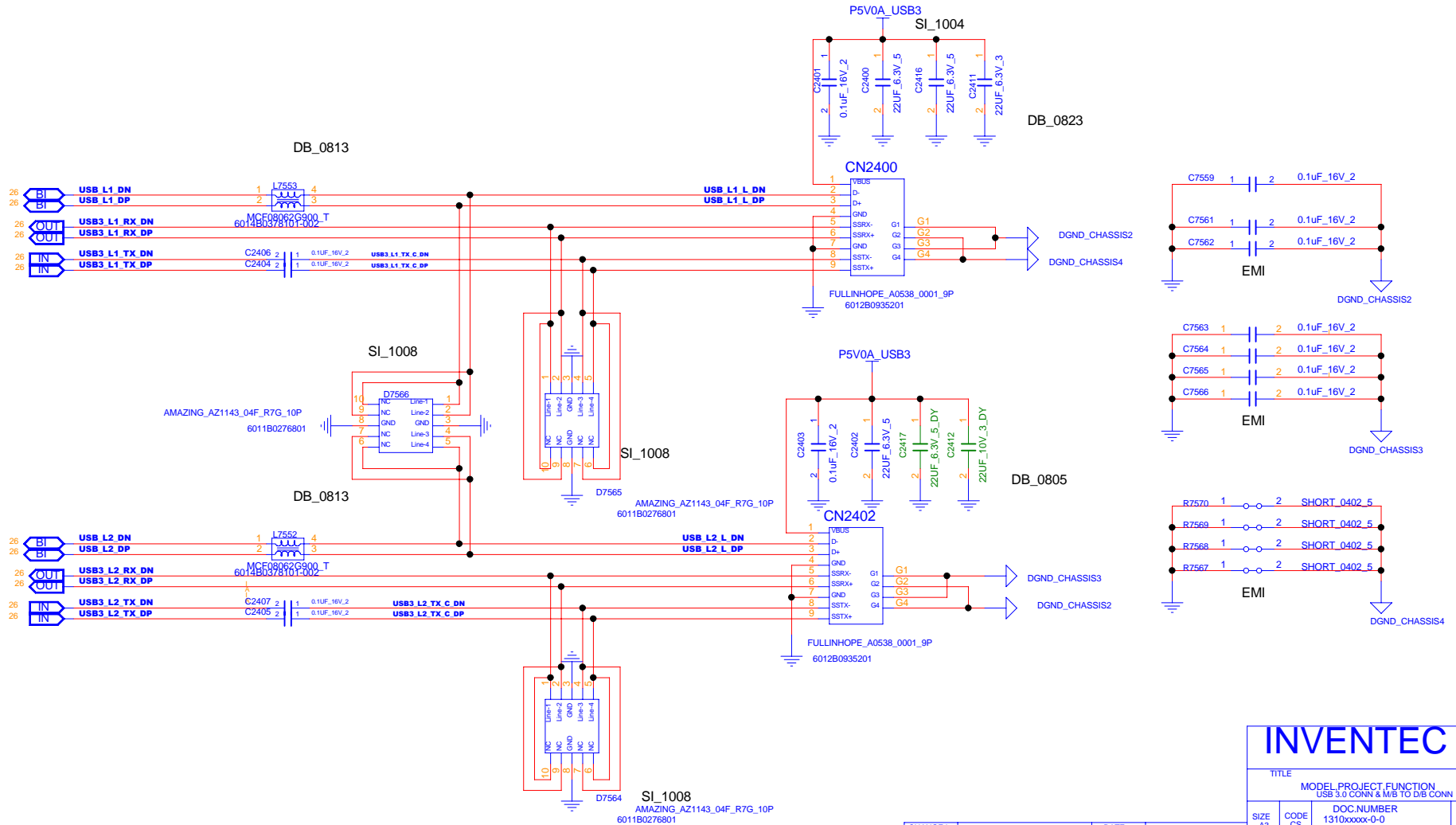
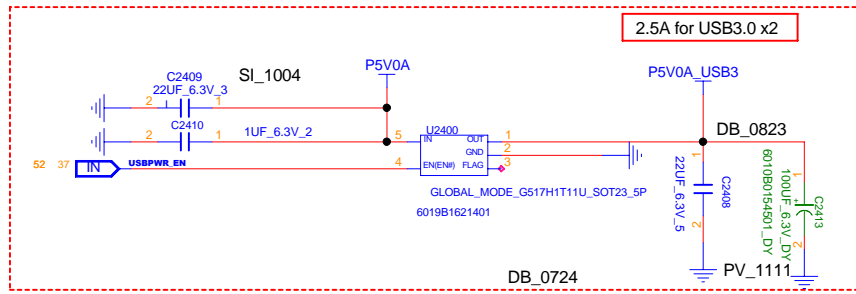
LOCATION 3000 ~ 3049





USB3.0

LOCATION 2400~2499
VER.08_20171119



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TITLE
MODEL PROJECT FUNCTION
USB 3.0 CONN & MIB TO DIB CONN

SIZE A3 CODE CS DOC NUMBER 1310xxxx-0-0 REV X01

CHANGE by XXX DATE PCB VER X01 RCT-2002

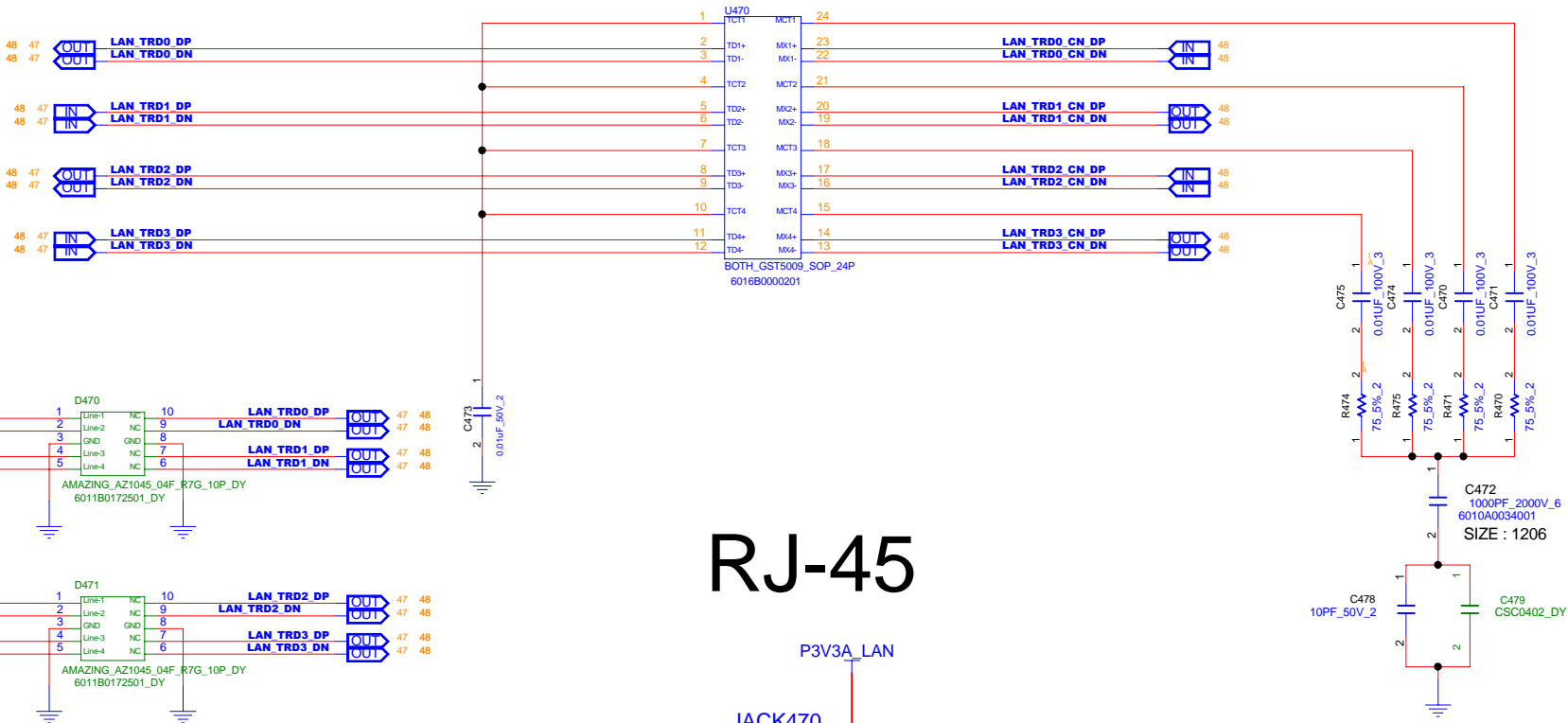
SHEET 44 of 75

LAN (Transformer & RJ45)

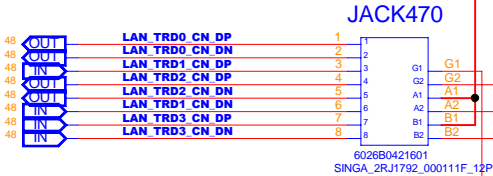
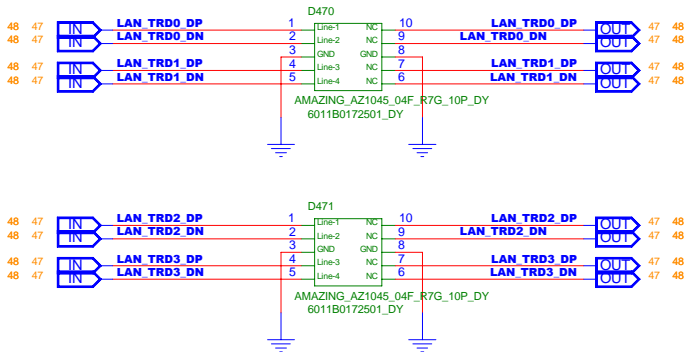
Location 470 ~ 499
VER.05_20171107

For 10/100/1000 LAN GIGA main BOM change to 6016B0000201

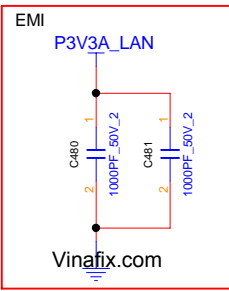
10/100/1000 MAIN====> BOTHHAND P/N : 6016B0000201 GST5009
10/100/1000 2ND====> UDE P/N : 6016B0022201 L22N001-0



RJ-45



NODE	COLOR	
A1(+)	A2(-)	AMBER
B1(+)	B2(-)	WHITE



INVENTEC

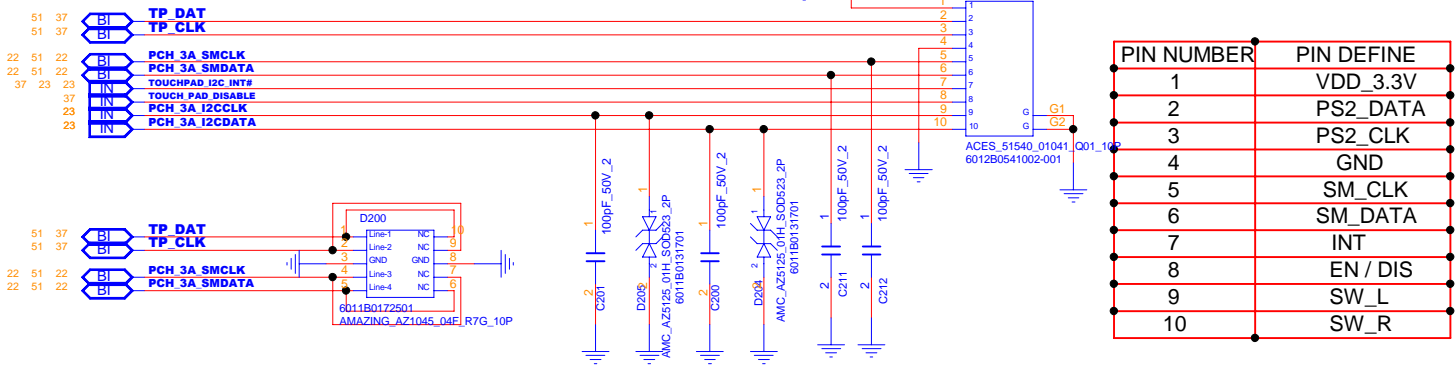
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

TITLE	MODEL PROJECT FUNCTION	DOC NUMBER	REV
SIZE	A3	CS	X01
SHEET	48	of	75

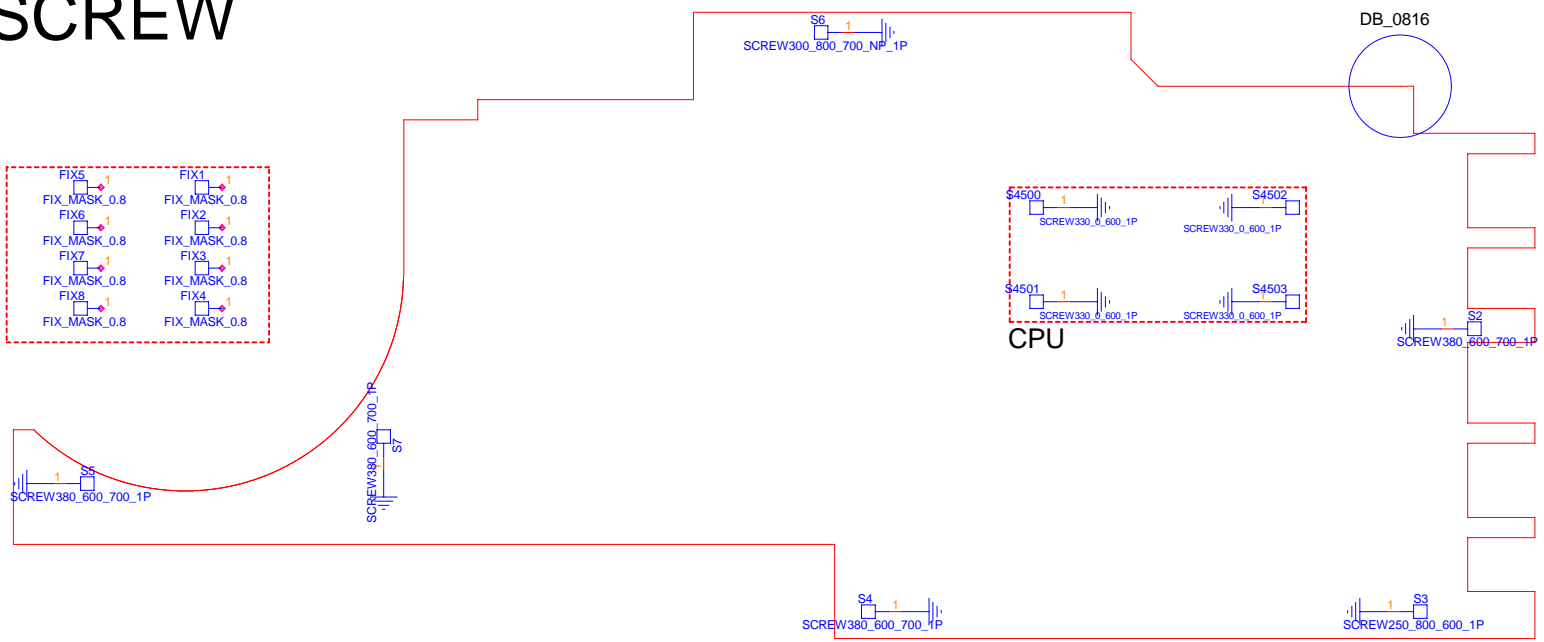
TOUCHPAD MODULE CONN

FOR INTEL USE

VER.14_20171119



SCREW



INVENTEC

TITLE
MODEL PROJECT FUNCTION
POWER BUTTON

SIZE A3 CODE CS DOC NUMBER 1310xxxx-0-0 REV X01

CHANGE by XXX DATE PCB VER X001 PCB X001

SHEET of 51 75

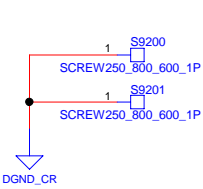
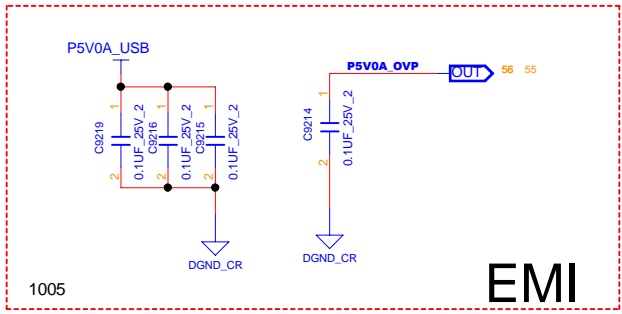
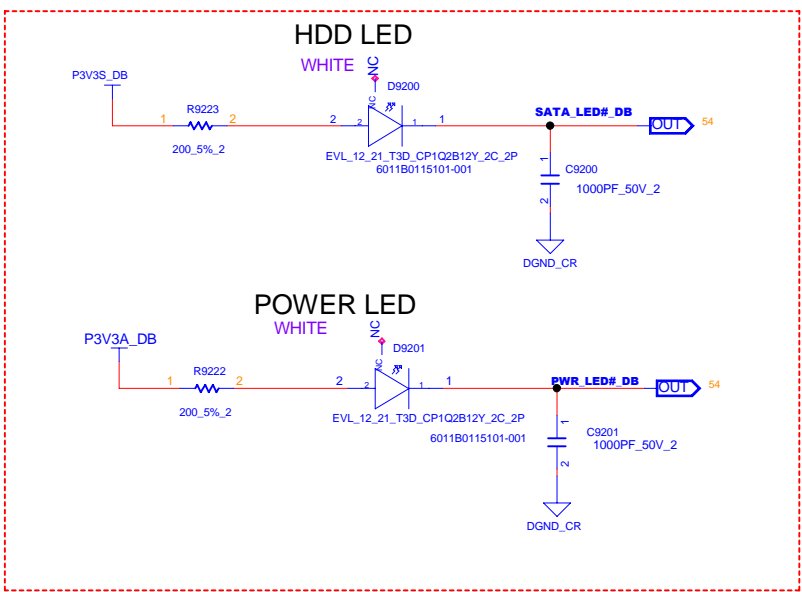
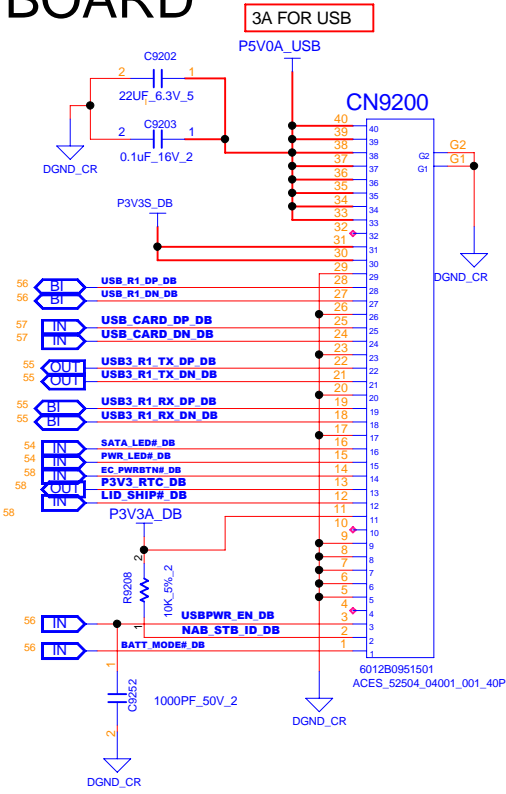
Small Board

- 1.USB & CR FOR NARROW BORDER (LOCATION : 9200)
- 2.USB & CR FOR STANDARD BORDER (LOCATION : 9600)
3. PICK BUTTON BOARD (LOCATION : 9300)

CARDREADER USB BOARD

FOR NARROW BORDER USE

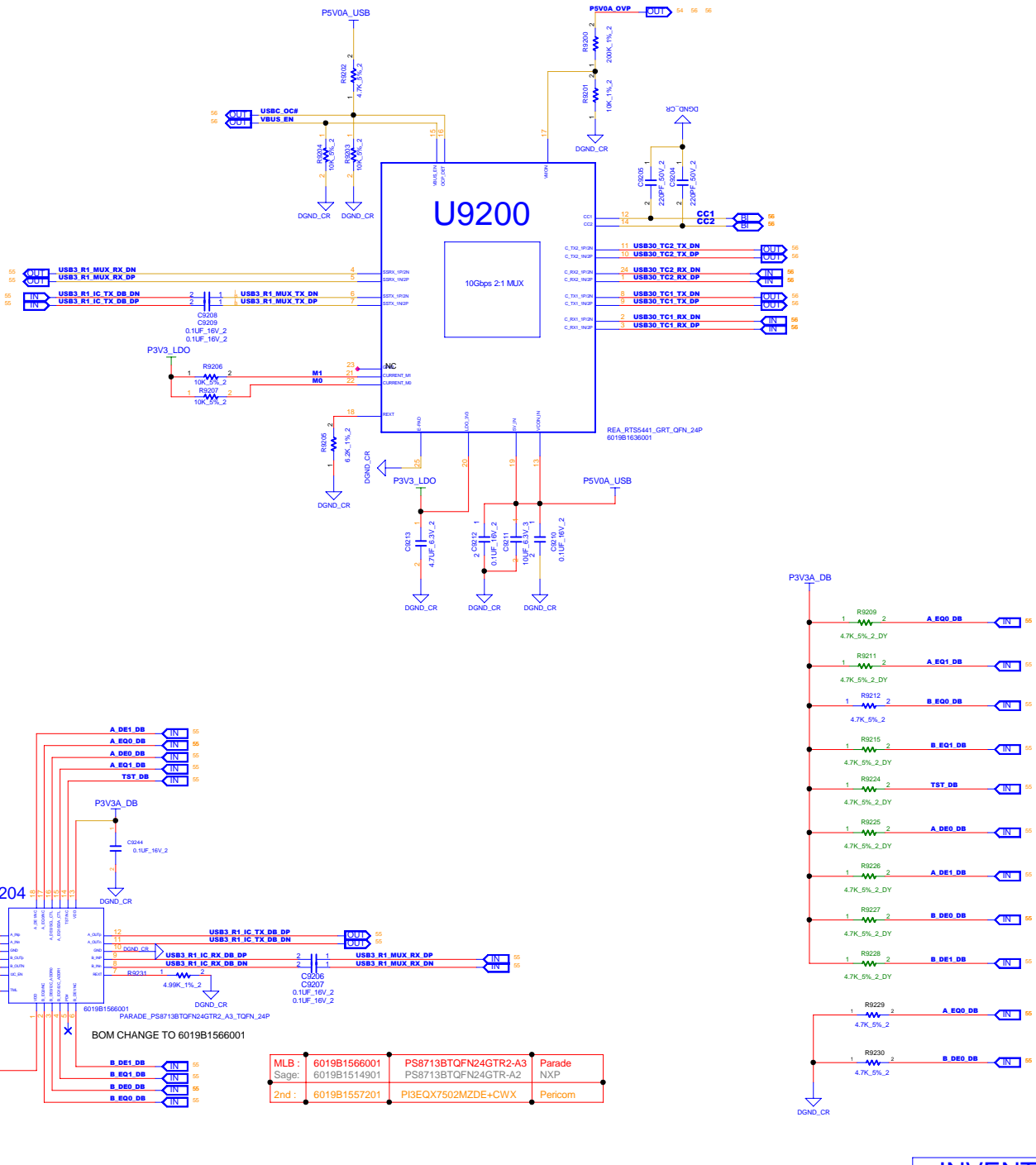
VER.09_20171109



FIX_MASK_0.8	FIX_MASK_0.8	FIX_MASK_0.8	FIX_MASK_0.8
FIX_MASK_0.8	FIX_MASK_0.8	FIX_MASK_0.8	FIX_MASK_0.8
FIX_MASK_0.8	FIX_MASK_0.8	FIX_MASK_0.8	FIX_MASK_0.8
FIX_MASK_0.8	FIX_MASK_0.8	FIX_MASK_0.8	FIX_MASK_0.8
FIX_MASK_0.8	FIX_MASK_0.8	FIX_MASK_0.8	FIX_MASK_0.8

USB3.0 MUX

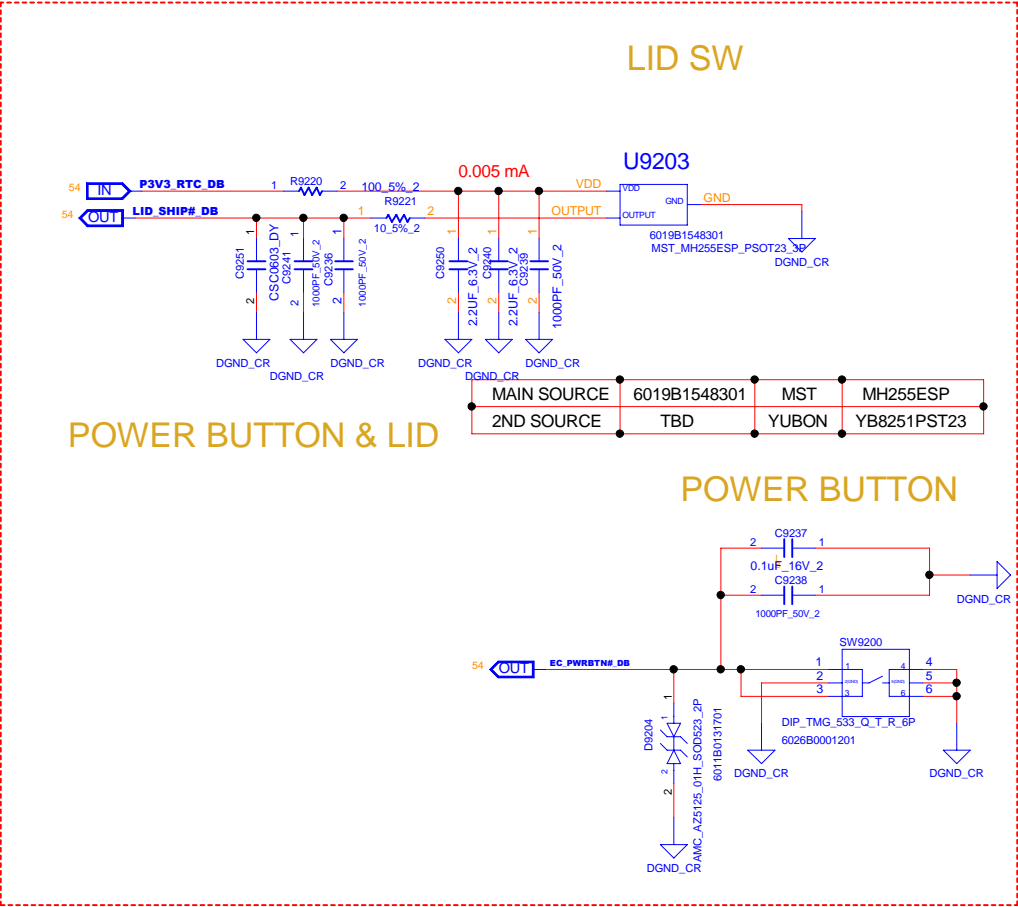
FOR NARROW BORDER USE
VER.02_20170919



LID SW & POWER BUTTON

FOR NARROW BORDER USE

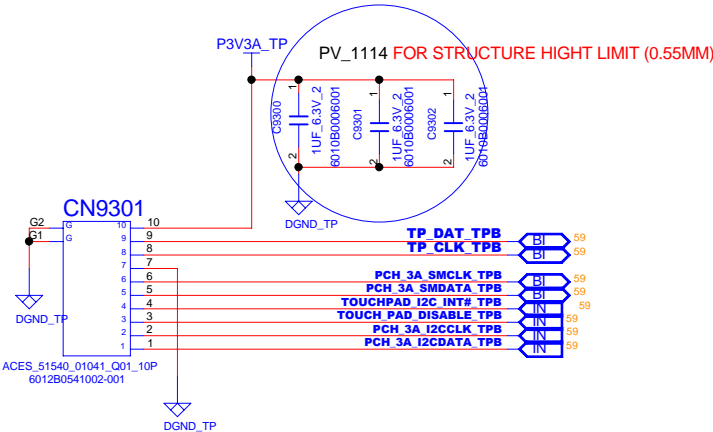
VER.07_20171120



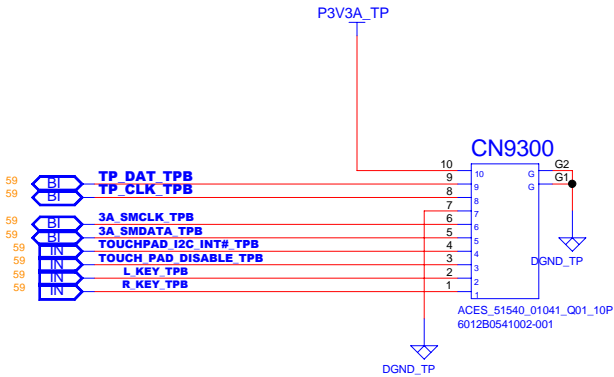
PICK BUTTON (TYPE_C)

TOUCHPAD R / L BOARD

VER.03_20171119

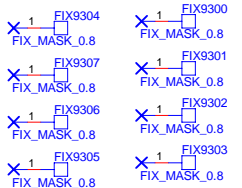
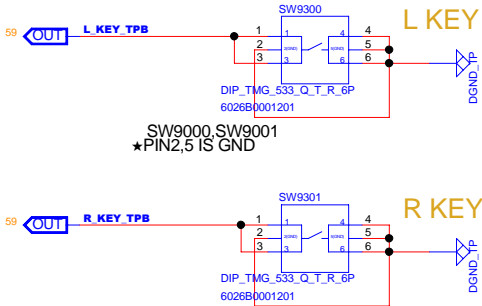
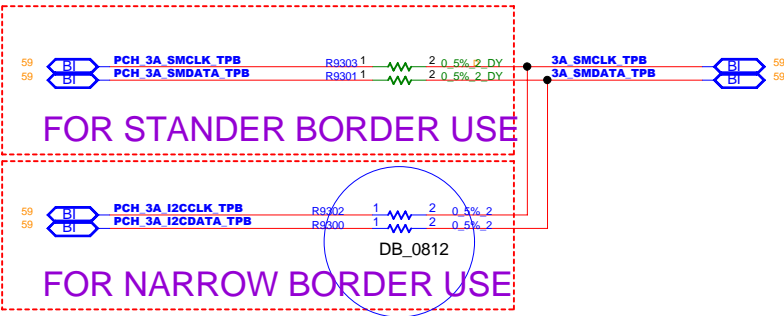


TO MAIN BOARD



TO TP MODULE

PIN DEFINE	PIN NUMBER
VDD_3.3V	1
PS2_DATA	2
PS2_CLK	3
GND	4
SM_CLK	5
SM_DATA	6
INT	7
EN / DIS	8
SW_L	9
SW_R	10



INVENTEC

TITLE	MODEL PROJECT FUNCTION	DOC NUMBER	REV
SIZE A3	CODE CS	1310xxxx-0-0	X01
SHEET	59 of 75		

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NOTES:
1.HSF Property:Comply iSupplier system HSF property attribute up-to-date value.

AMD R19M-M18/30 18W

GDDR52PCSX64BITX256MX32

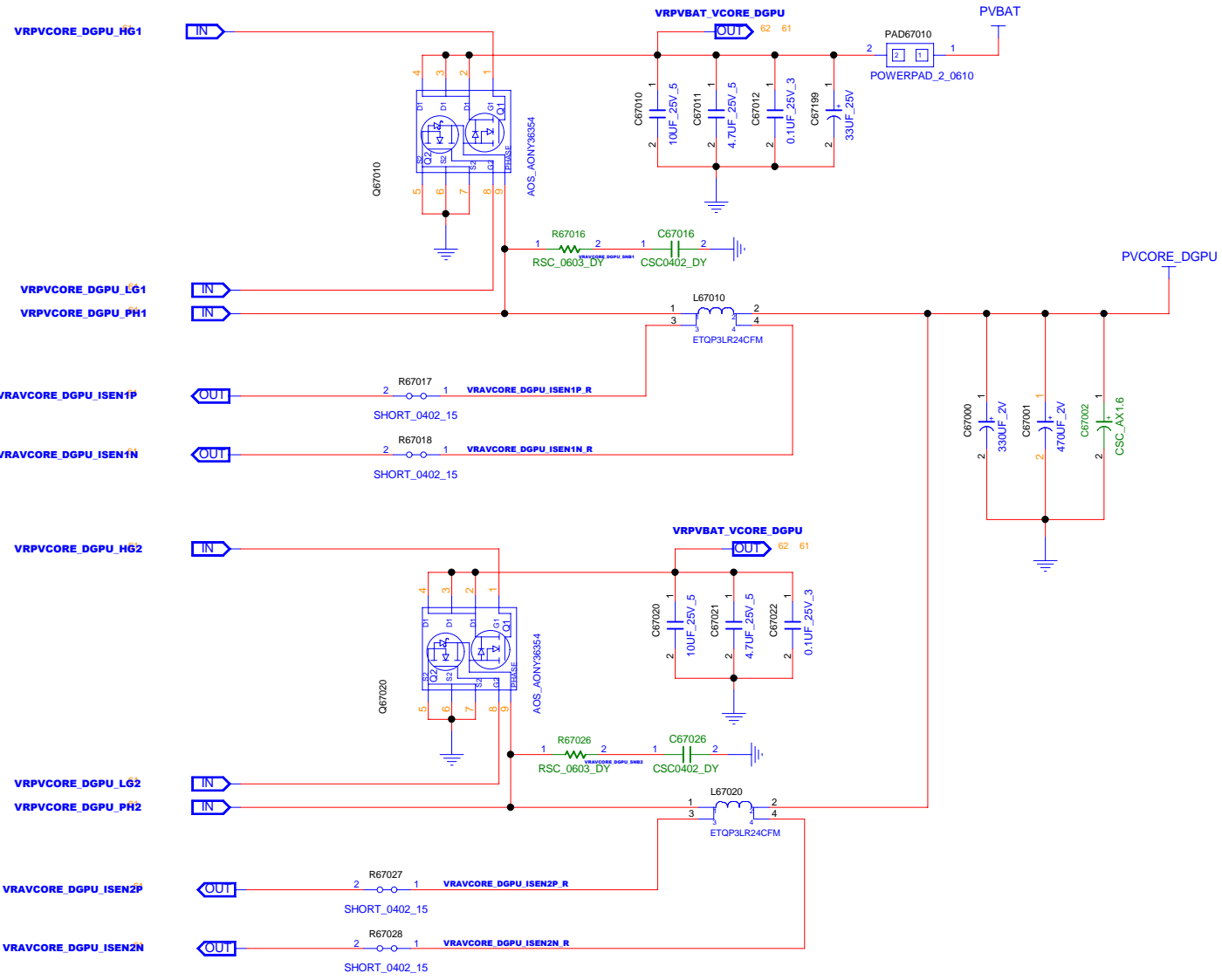
2019.11.14

R19M-M18-30 PART NUMBER TABLE

	U5001
M18-30	6019B1961001

R19M-M18-30 /70 BOOT VID

Boot-VID Code		
SVC	SVD	Voltage Selected (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



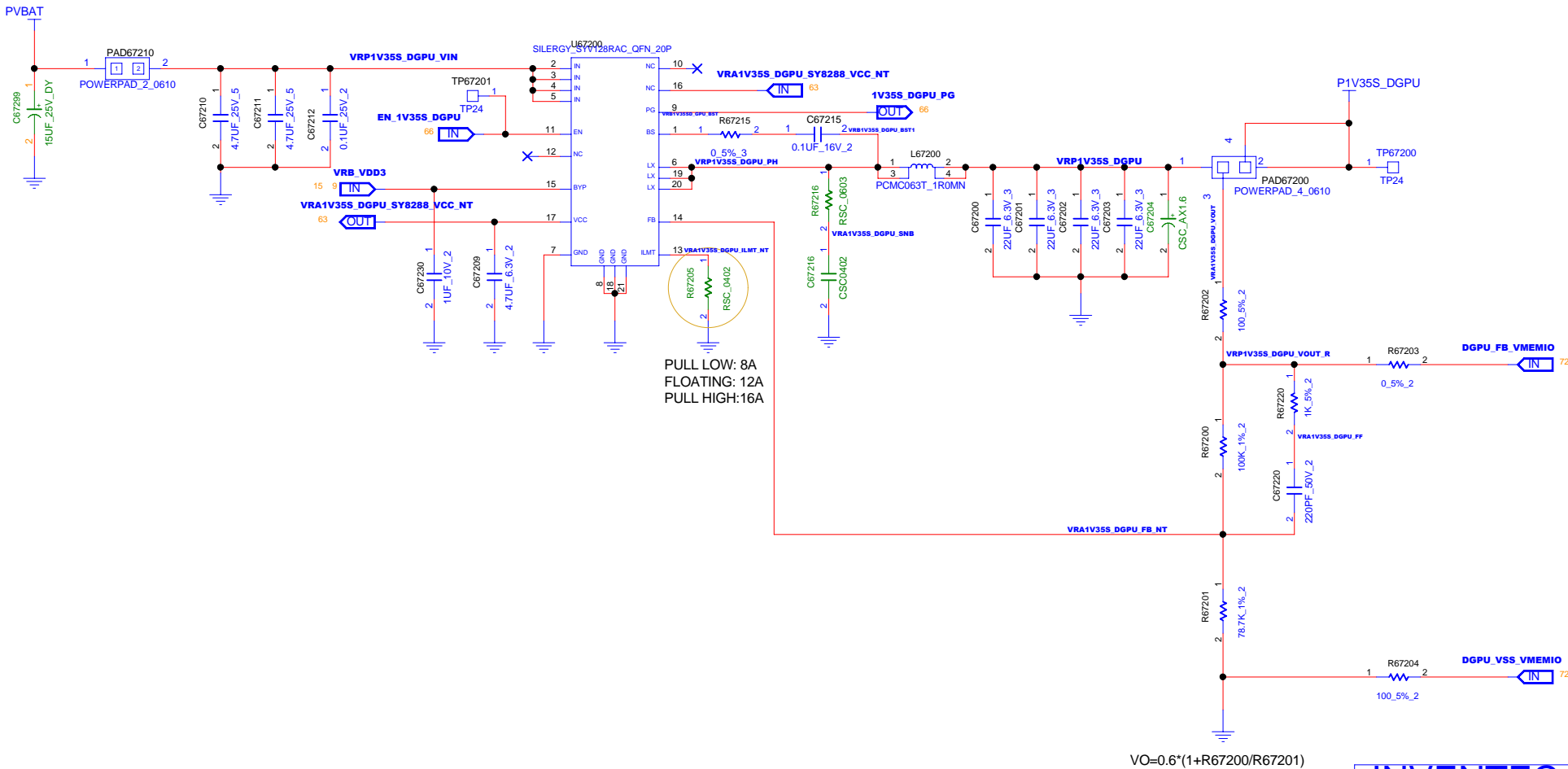
Vinafix.com

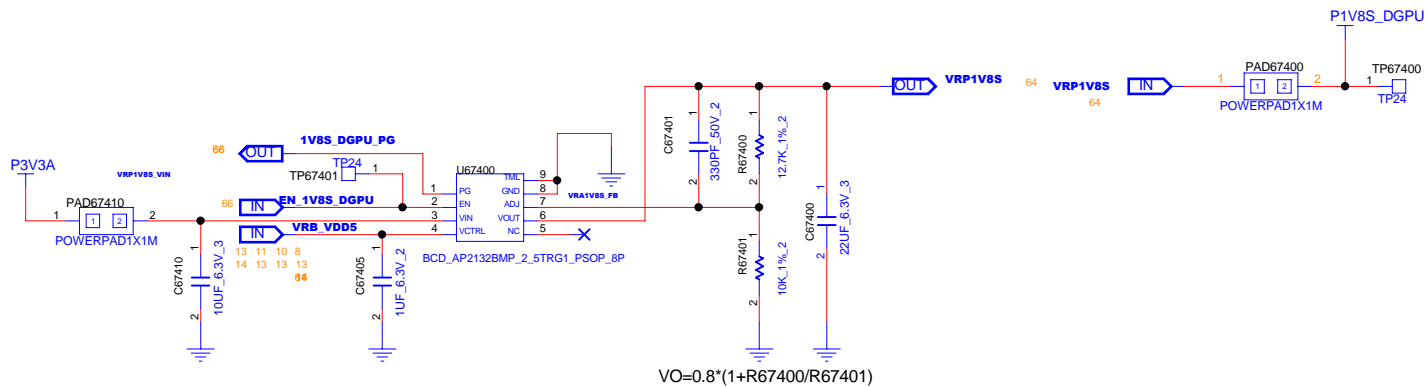
INVENTEC

TITLE
MODEL PROJECT FUNCTION
Block Diagram

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET	62	of 75	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX





56108_1.02_eng-R19M-M18-30.pdf * - Foxit Reader

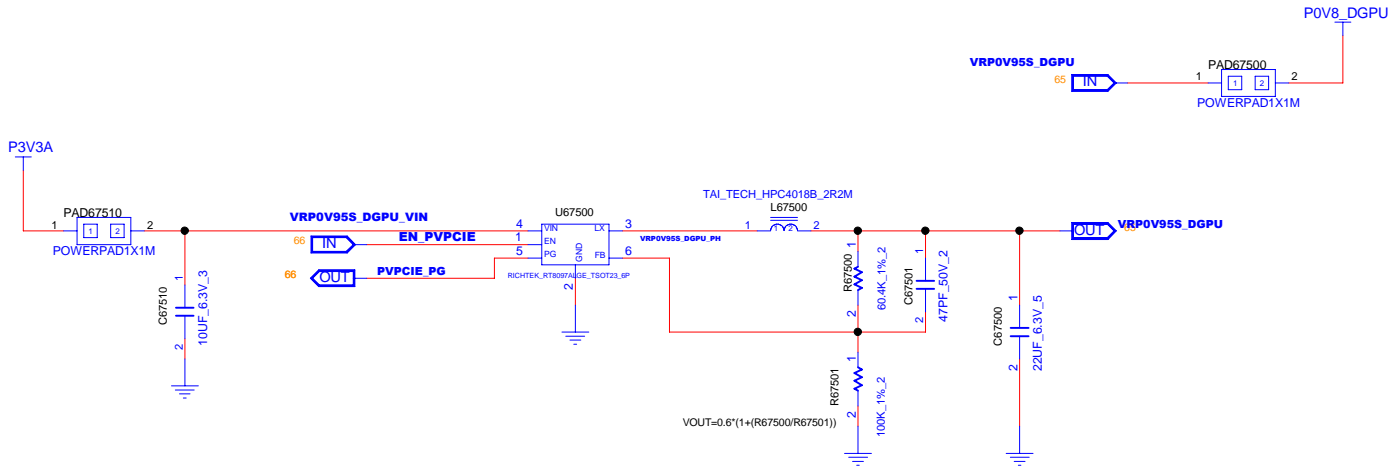
HOMI COM VIEW FORM PROT SHAR FOXI HELP

Find

Start

56108_1.02_eng-R19...

VDD_08	0.95 V	± 3%	± 3%	2 A (TDC)	6, 8
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INVENTEC

TITLE
MODEL PROJECT FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
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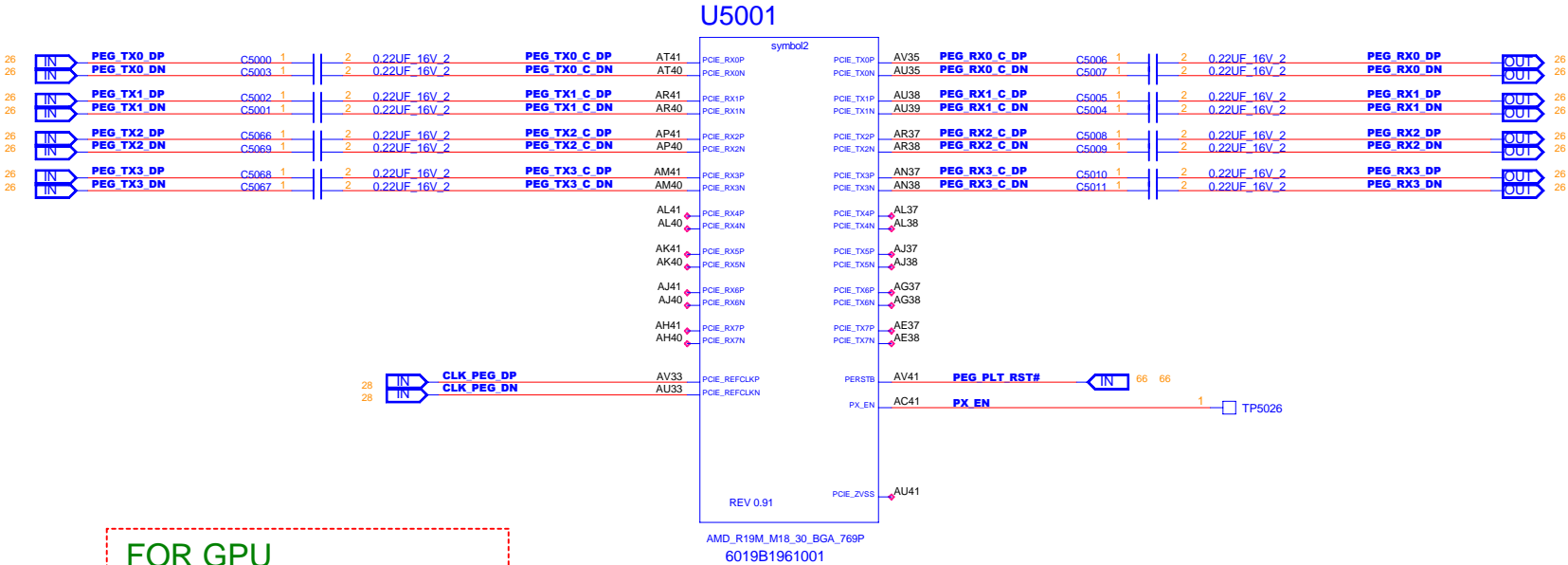
CHANGE by PCB P/N	XXX 60xxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
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SHEET 65 of 75

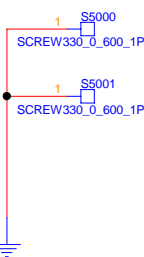
GPU PCI-E

U5001
R19M-M18-30
216-0915020
6019B1961001

PLEASE NOTE!! THIS SYMBOL IS THE SAME PIN DEFINE AS R19M-M18-70,BUT IT'S NOT R19M-M18-30.
THE CIRCUIT STILL NEEDS TO REFER TO THE R19M-M18-30 SPECIFICATION



FOR GPU



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TITLE
MODEL PROJECT FUNCTION
POLARIS-1

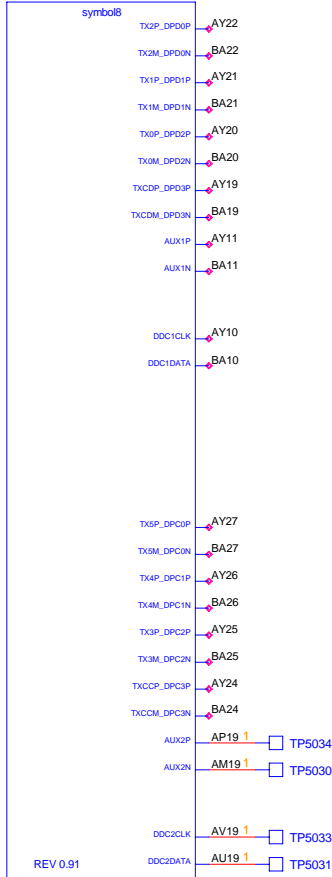
SIZE A3 CODE CS DOC NUMBER 1310xxxx-0-0 REV X01

CHANGE by XXX DATE 21-OCT-2002
PCB P/N 60xxxxxxxxx PCB VER XXX

SHEET 67 of 75

GPU VGA / LVDS / DVI / HDMI / DP

U5001



AMD_R19M_M18_30_BGA_769P

6019B1961001

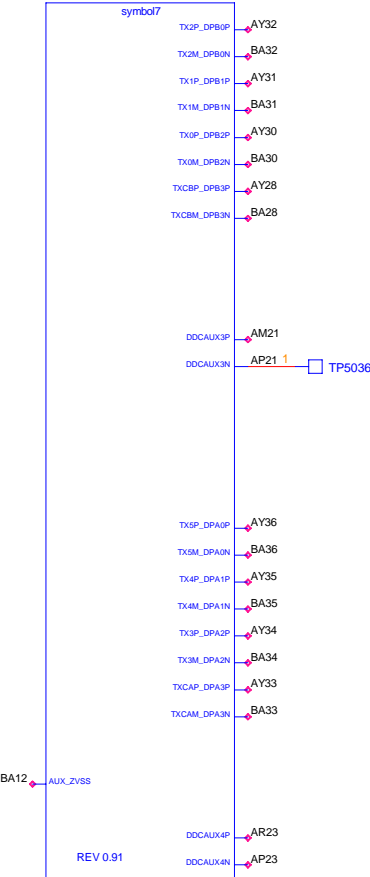
U5001



AMD_R19M_M18_30_BGA_769P

6019B1961001

U5001



AMD_R19M_M18_30_BGA_769P

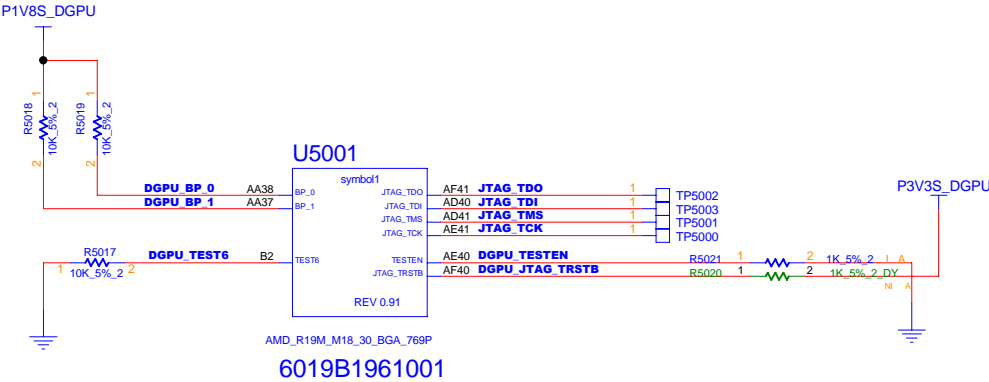
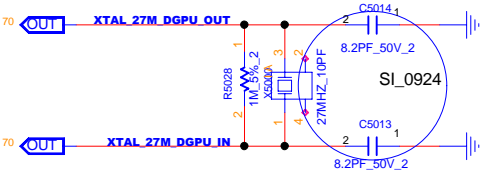
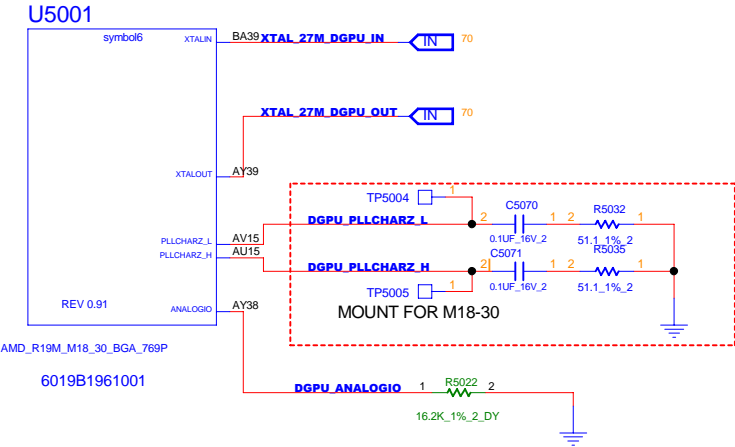
6019B1961001

INVENTEC

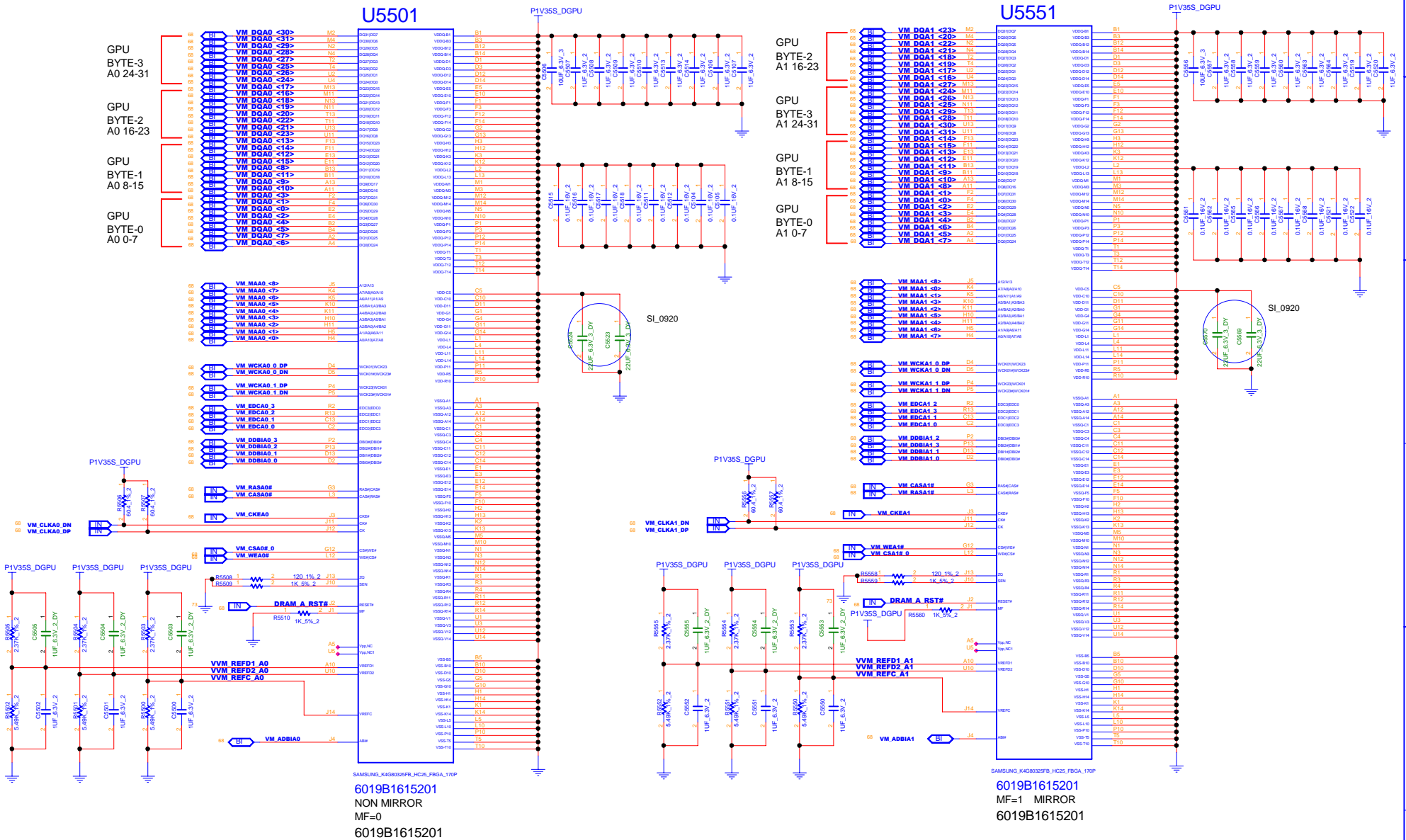
TITLE
MODEL PROJECT FUNCTION
POLARIS-3

SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET		69 of 75	

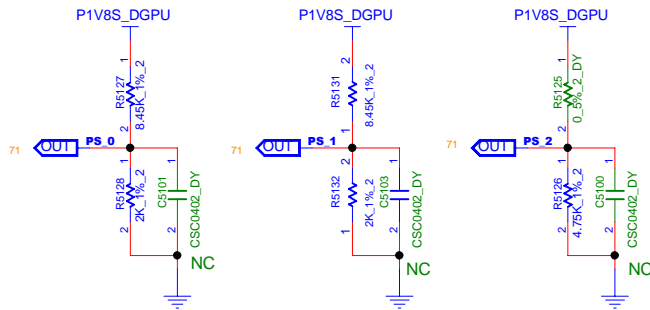
GPU-CLOCK/JTAG



GDDR5 VRAM



R19M-M18-30VVRAM ID



PS0[5:1]	1	1	0	0	1
PS1[5:1]	1	1	0	0	1
PS2[5:1]	1	1	0	0	0
PS3[5:1]	1	1	PS3[3]	PS3[2]	PS3[1]

APERTURE MEMORY SIZE IS 256K
R5127 IS 8.45K OHM \ R5128 IS 2K OHM

MULTI LEVEL PIN STRAP (MLPS)
FOR R_PU_X AND R_PD_X AND C_X, SELECTION
REFER TO AN.MEN.X1
PARTS FOR MLPS SHOULD BE PLACED CLOSE TO ASIC
THE TOTAL RESISTANCE OF TRACE SHOULD BE LESS THAN 3 OHM

R_PU	R_PD	BITS[3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

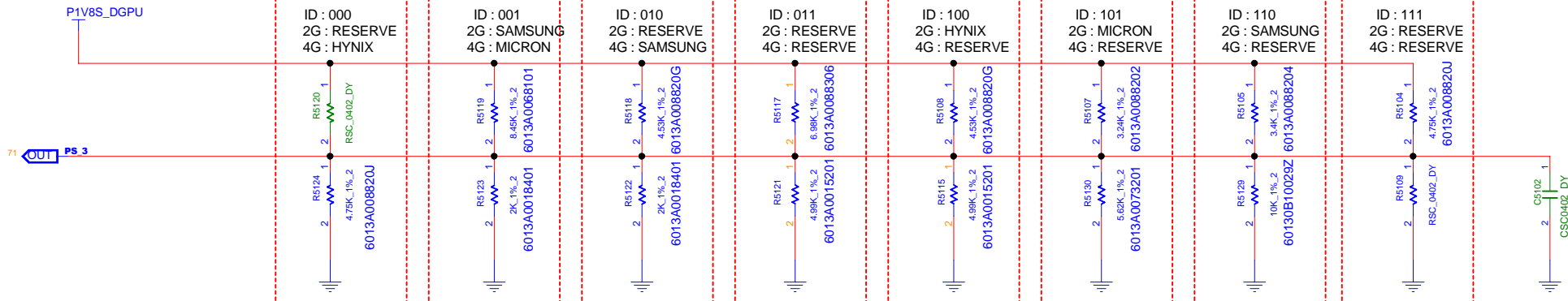
2K_1% : 6013A0018401
3.24K_1% : 6013A0088202
3.4K_1% : 6013A0088204
4.53K_1% : 6013A008820G
4.75K_1% : 6013A008820J
4.99K_1% : 6013A0015201
5.62K_1% : 6013A0073201
6.98K_1% : 6013A0088306
8.45K_1% : 6013A0068101
10K_1% : 60130B10029Z

NOTE: 0402 1% RESISTORS ARE REQUIRED.

CAPACITOR VALUE (NF)	BITS [5:4]
680	00
82	01
10	10
NC	11

R5120, R5119, R5118, R5117, R5108, R5107, R5105, R5104
ARE COLAY WITH SAME POSITION

R5124, R5123, R5122, R5121, R5115, R5130, R5129, R5109
ARE COLAY WITH SAME POSITION

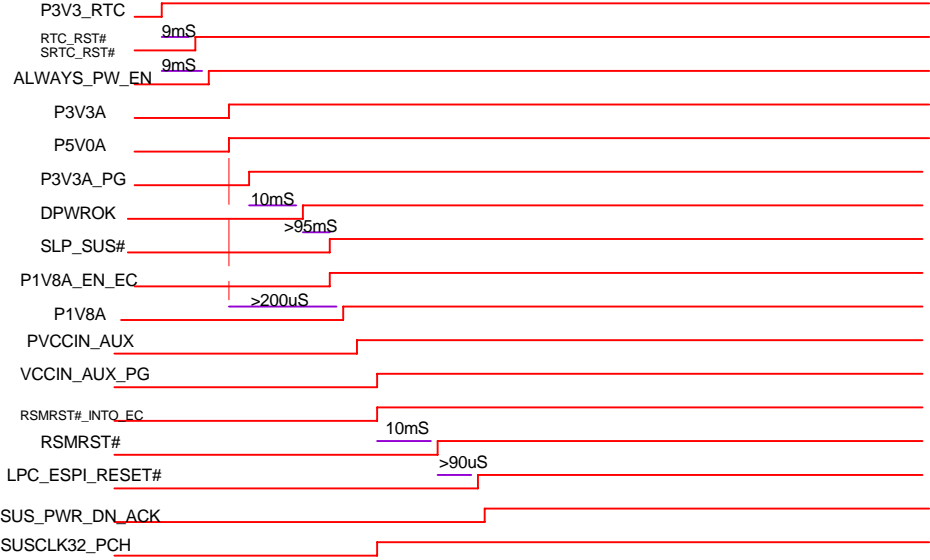


VRAM ID TABLE (256M X 32) TWO PIECES CHIP

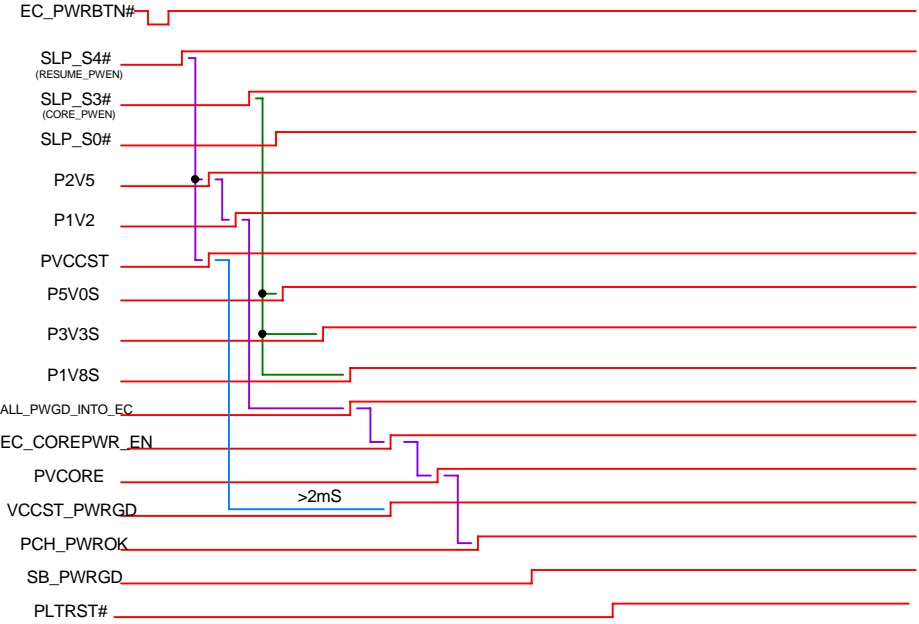
R_PU	R_PD	PS_3[3]	PS_3[2]	PS_3[1]	VENDER	IEC P/N	CONFIGURATION	VENDER P/N
NC (R5120)	4.75K (R5124)	0	0	0	RESERVE		256M X 32	
8.45K (R5119)	2K (R5123)	0	0	1	Samsung	6019B1926601	256M X 32	K4G80325FC-HC25 *
4.53K (R5118)	2K (R5122)	0	1	0	RESERVE		256M X 32	
6.98K (R5117)	4.99K (R5121)	0	1	1	Micron	6019B1721101	256M X 32	MT51J256M32HF-80:B B *
4.53K (R5108)	4.99K (R5115)	1	0	0	Hynix	6019B1542101 6019B1615301	256M X 32	H5GC8H24MJR-R0C H5GQ8H24MJR-R4C
3.24K (R5107)	5.62K (R5130)	1	0	1	Micron	6019B1486001	256M X 32	MT51J256M32HF-70:A
3.4K (R5105)	10K (R5129)	1	1	0	Samsung	6019B1485901 6019B1615201	256M X 32	K4G80325FB-HC28 K4G80325FB-HC25
4.75K (R5104)	NC (R5109)	1	1	1	Hynix	6019B1723701	256M X 32	H5GC8H24AJR-R2C A *

POWER SEQUENCE

G3 to S5



S5 to S0



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TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002	SIZE A3	CODE CS	DOC NUMBER	REV
PCB P/N	60xxxxxxxxxx	PCB VER	XXX	SHEET	75 of 75	1310xxxxx-0-0	X01